Hardware Algorithm for Static and Dynamic Rams Testing.

Mofreh Mohamed
Associate Professor of Computers and Control Department, Faculty of Engineering, Mansoura University, Mansoura, Egypt., dr_mofreh@mans.edu.eg

Aida El-Gwad
Computers and Control Department, Faculty of Engineering, Mansoura University, Mansoura, Egypt.

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HARDWARE ALGORITHM FOR STATIC
AND
DYNAMIC RAMs TESTING

طريقة مكونات ماديه لاختبار الذاكره
الاستاتيكية و الديناميكيه

MOFREH M. SALEM   AIDA O. A. EL-GWAD

Computers and control Dept., Faculty of engineering
EL-Mansoura Univeristy, EL-Mansoura, Egypt

ملخص

وحدة الذاكرة (خصوصا ذاكرة الوصول العشوائي   ) تستخدم في كل عمليات الحاسب بوحدة التشغيل المركزية أو الادخال والاخراج. لذلك فإن اختبار مثل هذا النوع من الذاكرة أصبح مشكلة هامة حظيت بالاهتمام في كثير من الابحاث. وهناك طرق قد تم اقتراحها في أبحاث سابقة لاختبار الذاكرة الساكنة باستخدام المكونات البرمجية أو المكونات المادية . . . ومعظم هذه الطرق يعيبها طول الزمن اللازم لاجراء مثل هذا الاختبار وكذلك فإن هذه الطرق تستطيع فقط اكتشاف الاخطاء المعروفة سابقا.

لذلك كان هذا البحث حيث يقترح طريقة جديدة تستخدم المكونات المادية في اختبار الذاكرة الديناميكية.

ويحتوى البحث على شرح تفصيلى للطريقة المقترحة ودوائرها ونتائج الاختبارات المعملية التى أثبتت كفاءة الطريقة.

ABSTARCT

The main purpose of this paper is to establish an efficient hardware algorithm for static and dynamic RAMs testing. The paper discribes the analytical formulation, the hardware realization, and the experimental results of the propsed algorithm when used in testing RAMs as this type of RAMs are widely used .

INTRODUCTION

Memory unit specially the RAM type interacts with CPU and I/O devices and always used in all computer operations. Therefore testing of RAM's is an important problem since RAM's are widely used. Such test may be software or hardware.

Many algorithms have been developed for functional testing of RAM's [1-6]. However most of them require a time increasing more than proportionally to the number of cells. This may become a crucial point due to enlarging of scale integration. Furthermore, it becomes very difficult and may be even impossible to find such that algorithm, when multiple fault is present in the RAM. An alternative solution is the random testing to detect faults resulted from : short cell, open cell, short address and disturbed cells. In general there are different test patterns they are; all zero all one, checkerboard, marching, and walking test patterns. In this case a sequence of random patterns is simultaneously applied to a RAM under test and compare the output of this

RAM to reference memory. The ability of a given test pattern to detect a fault depends on the design geometry, and output of the memory cells. So, these methods are widely applicable since the test pattern generation is independent of the predescribed set of faults. However, for any fault, there is no certainty about the detection of this particular fault. Also, the probability that this fault is detected if it is present in the circuit, is an increasing function of the number of random patterns.

Static RAM the ideal approach for microcomputer because it is fast and it dos not need refreshing circuitry. However there are tow good reasons for using dynamic RAM, first the amount of circuit board space used for static RAM is three times that used for dynamic RAM, i.e, three dynamic storage cells can fit into about the same space as one static storage cell. The second reason for using dynamic RAM is the power dissipation (the amount of power required to operate the memory device, in watts per storge cell), it requires from 4 to 100 microwatts per cell. While the power dissipation for static RAM range from 100 to 400 microwatts per cell. Naturally, we can not forget the additional circuitry needed to handle memory refresh.

Dynamic RAM is available in different size memory package ranging from 1 K bit to 64 M bit.This paper presents a hardware algorithm to test static and dynamic RAMs. The algorithm is described with respect to a 64 K bit as it is one of the more popular RAM package. In this algorithm each address of the RAM is tested through writing "0" into it, change the mode of the RAM to READ mode and check if there is "1" in this location, write "1" in the same location and read it to check if there is "0" and so on with the rest of addresses. Finally, the paper includes the complete description of the hardware realization and the conulsion of the experimental results. It shows that the proposed tester for static and dynamic RAM's exhibits the most attractive property for practical implementation.

CIRCUIT DESIGN AND EXPERIMENTAL RESULTS

The 64 Kbit RAM requires 16 bit address to decode one of 2^{16} storage cell locations. Due to reducing the number of pins on the RAM chip, the memory address are normally divided into two steps. The first 8 bits of the address are sent when the control signal of row address strobe (RAS) is enabled and the subsequence 8 bits are followed when the control signal of column address strobe (CAS) is enabled high. So, there is only 8 address pins available on the ship. However, testing of a such chip requires 16 address lines to access all 64 K bit. Also dynamic RAM must be refreched at least once every 2 millseconds to keep the information in it. The refreshing is very important in dynamic RAM testing however it is complex. To avoid this complextiy we proposed some modification.

The hardware realization for one of the most common test patterns, to detect short and open cell's also to detect adjacent cell shorts in a 1 K bit static RAM (memory chip 2102) is shown in figure (1). Firstly aschmitt trigger inverter N12 is used as a simple oscillator with (0.22 MHz) this oscillator is used to drive 3-ripple binary coun ters (IC5, IC6, IC7) connected in cascade, this generate 12 bit binary output, first 10 bits are used to address the 1024 memory location in the 1 K bit (2102) static RAM, the last two bit (most significant) are used to feed the decoder (74155) as an input. This IC contains two (2-TO-4) decoders,in our circuit one of them used, the output lines of decoder at pines (9-10-11-12), pin 9 is used as data input of static RAM, pins 9 NANDed with 11 are used for (R/W) enable of static RAM,pin (10,11) connected to the indicating circuit, the indicating circuit contents of two IC 7400, 7414 from (N1 TO N6)in 7400 and from (N7 TO N12) in 7414 chip (the indicating circuit is used to control 2102 and test

logic). The static RAM chip which used in this circuit is "5257" is 4K bit static RAM which have 12 pins from A0 TO A11 to address 4 ö1024 memory location, but it is used as 1 K bit in stead of 2102, so it use only 10 pins from A0 to A9 to addresses 1024 memory location and ignore A10, A11 by this way the chip 5257 is used as 1 K bit. The output of the counter will be the input of the RAM chip and then every cell in the RAM must be addressed at every count pulse, the first ten output of the counter will generate the 1024 addresses of the memory, and the most two bits will generate four cases as shown:

				decoder pins		
	3	13	9	10	11	12
state 1	0	0	0	1	1	1
state 2	0	1	1	0	1	1
state 3	1	0	1	1	0	1
state 4	1	1	1	1	1	0

Assuming that initially all 12 outputs from the counter are low Then pins 3 and 13 are also low.

STATE   0 0

In this case pin 9 of decoder (which pulling data to the RAM) switched to logic "0" and pins 10, 11, 12 are switched to logic "1", where pin 9 is logic "0", pin 11 is logic "1"

Then output of   N1   is   1

　　　　　　N9   is   0

Via N1,N9 the RAM switched to the write mode,during the first 1024 counts all memory locations in RAM are setting to "0",pin 10 is "1" , pin 12 is "1" ,in this mode the output of gates as follow:-

N7	is	0
N8	is	0
N2	is	1
N3	is	1
N4	is	0
N11	is	1

Note : state of R (rest of flip flop)initially is logic 0, S(set of flip flop) is logic "1" (out of N11) then:

inp of F/F		output	
S	R	N5	N6
1	0	0	1

Where state of point A and B is logic "1", then D1 on ,D2 off
Then GREEN LED light. At the next count pin 13 of decoder is pulled "1" and pin 3 still in logic "0".

STATE   0 1

In this case pin 10 goes logic "0", and pins (9, 11, 12) goes   logic "1", pin 9 is "1", pin 11 is "1", then, output of N1 is "0",
　　　　　N9   is "1",

the RAM is switched to the read mode, all memory locations in RAM are red,if the RAM output pin 7 remains "0" during all the 1024 counts then, the green led will light, this is mean that it may be good,if any "1" appear at the output of the RAM this sets the flip-flop and the red led will light, this is mean that a short to Vcc at some cell and then the RAM is bad, and so on for the case (0 1) the RAM is switched to the write mode and the pin 9 of the decoder will pulling "1" to the input of the RAM through the next 1024 counts,then in the last case (1 1) the RAM is switched to the read mode if any "0" appear at the output of the RAM , then a red led will light this is mean that there are a short to GND and the RAM is bad, else a green led will light this mean that the RAM is good. After the fourth state then a count will begin from start, the complete test sequence take very little time, therefor to test any chip you plug it into its position in the circuit and switch on the power of the circuit, operate the rest switch (sr) if the green led lights this means that the IC is good.

In this paper the above described algorithm is modified so as it can be used to test a 64 K bit RAMs of both types ,static or dynamic. An external address multiplexer with signals RAS and CAS and the pervious information about row address latch and column address latch is used for such modification . Where the input of the multiplexer is the 16 bits address, while the output is the 8 address of row and in the next step the 8 address of column. This is done for every period of clock. Notice that the address multiplexer must first active the RAS line of the chip and simultaneously supply the address information provided by   lines A0—A7. So that the row addresses is latched, then address multiplexer must active the CAS line for the chip and supply the address information provided by A8—A15, so that the column address is latched.

The dynamic RAM must be refreshed at least once every tow milliseconds to keep the information in it. Refreshing requires that each row of RAM must be addressed at least once every tow milliseconds, during refreshing period we can not access the RAM and test operation should stopped once every two milliseconds to refresh bits in RAM and then return back to continue test operation. In the proposed circuit the count rat is "1/0.22 MHz" then to address every location in memory and write to it will need "1/0.22 * 2^{16} " milliseconds this time will be enough to losses information in the first cell if we go back to read it we will find something other, then refreshing is very important in our circuit in the case of testing dynamic RAM but its complex, to avoid this complexity we proposed some modification so we do not need to the refreshing operation the idea is very simple where in the modified circuit while addressing the first cell the RAM will be in write mode and the input will be "0" then mode will be change to read mode at the same time, if the output of RAM was "0" the green led lights, if the output was "1' the red led lights.Then address will change to next address and so on...

The circuit shown in fig. (2) gives the proposed hardware realization of a 64 K bit dynamic RAM memory location chip "4164". The idea of testing depending on making read/write process to the RAM as follow. Firstly, schmitt trigger inverter is used as a simple oscillator with" 0.22 MHz". This oscillator is used to drive five ripple counter "7493" with 20 bits address, the first two address b0, b1 is used as input for decoder bins, from b2 to b17 are used for input to 74158 chip multiplexer (to generate the address of 64 K bit). In the first count the output of coun ter is "0" for all lines if we take b0, b1 as input for decoder this input gives 4 states (write a "0", read "0", write"1",and read "1") at the same time the lines from b0 to b17 still "at the same address i.e. we read and write for one cell of memory loca tion at the same address. The process is repeated until all cells are tested.

CONCLUSION

This paper has discussed an efficient technique to speed up the RAM test algorithm. The experimental results confirm that the new technique has several advantages for practical Implementation.

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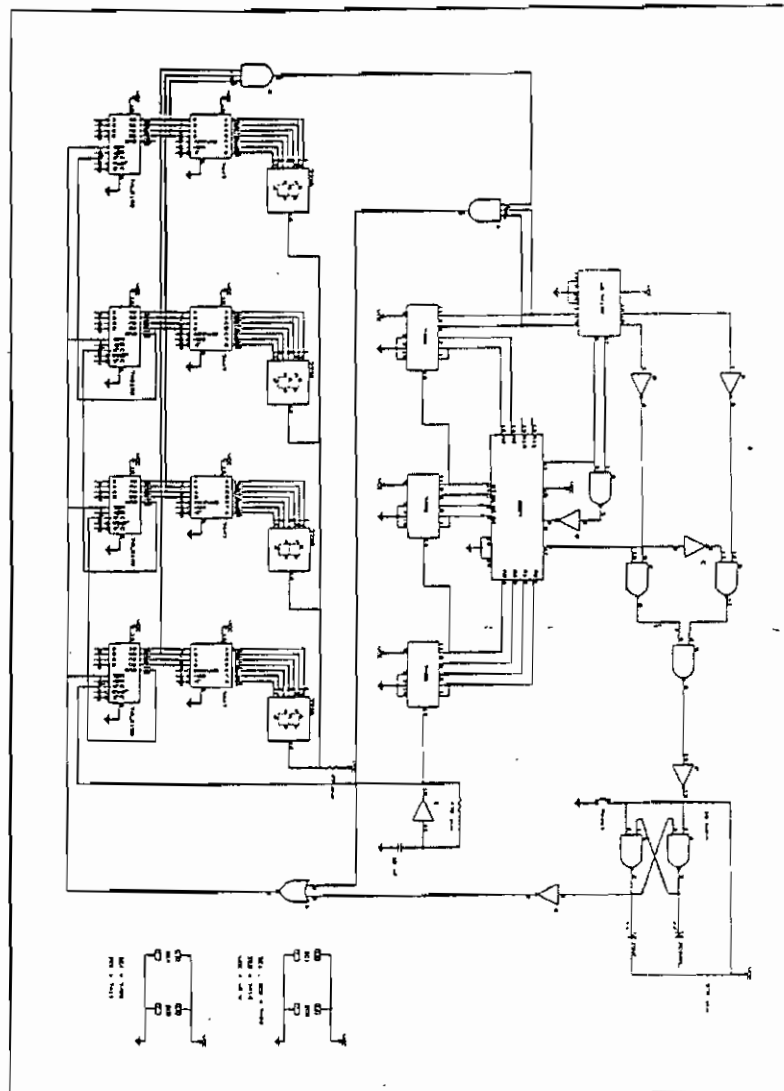   No.5 ,pp 637-650 May, 1989.

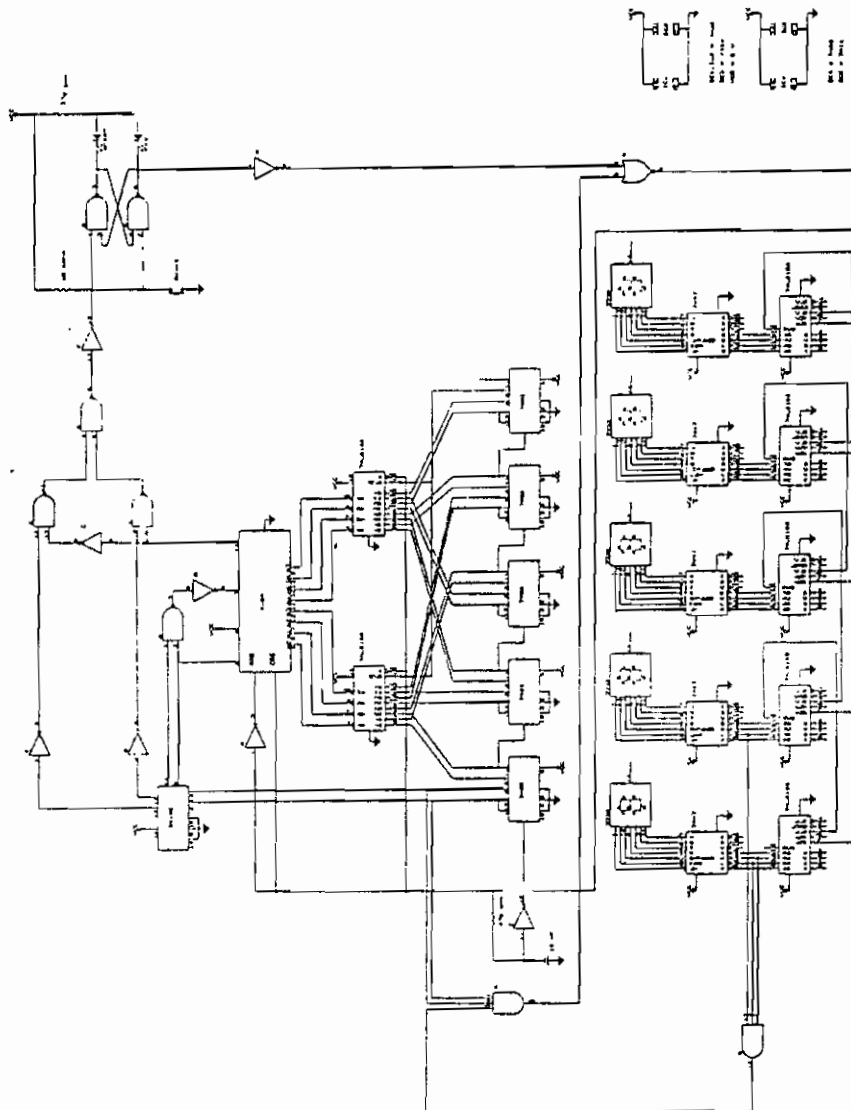Figure (1) : Circuit description of 1 K bit static RAM

Figure (2) : Circuit description of 64 K bit dynamic RAM