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# A 80 MS/S CMOS Sample-and-Hold Current Mode Circuit Using Double Sampling.

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# A 80 MS/S CMOS SAMPLE-AND-HOLD CURRENT MODE CIRCUIT USING DOUBLE SAMPLING

تصميم دائرة من نوع CMOS لاخذ عينات من الموجات بسرعة 80 ميجا عينة فى الثانية
بنظام التيار وباستخدام معدل تعيين مزدوج

**Hamed Elsimary,**
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**خلاصة :**

يقدم هذا البحث تصميما لدائرة الكترونية متكاملة باستخدام تكنولوجيا CMOS وتعمل هذه الدائرة التي تقوم بأخذ عينات من الموجـــات التناظرية المراد تحويلها الى رقمية بنظام التيار. وتتسم هذه الدائرة بانها تقوم بأخذ عدد مضاعف من العينات في نفس الزمن وذلك بحـتى ضعف المعدل العادي ولان بـ معدل استهلاك للقدرة وتتسم هذه الدائرة بانها ايضا بكونها كاملة التباين أي انها ذات مخرجين كل منهما عكس الأخر حتى يمكن تلاشي و ازالة الشوشرة الناتجة عن عملية أخذ عينات الدوحات وقد تم تمثيل و عرض نتائج الدائرة من خلال هذا البحث

**Abstract.** A fully differential CMOS sample and hold circuit (S/H) in current mode using double sampling technique is presented. Double sampling technique, gives a factor of two increase in the sampling rate while maintaining comparable power consumption and circuit complexity in comparison with the conventional S/H configuration. A precise current mirror circuit with low input impedance is adopted. A fully differential configuration for placing the switches were used to cancel the sample switches feed-through error. Also, the clock controlling the sample switches is boosted so as to make their on resistance low. The circuit is designed and simulated in 0.5 μm CMOS technology using BSIM3v3 device parameters. Simulation results show 10-bit operation at the sampling rate of 80 M sample/sec with 10mW power dissipation at 3V supply.

**Keywords:** Sample and hold circuits, current mode, double sampling.

## 1. Introduction

In most Analog to Digital converters A/Ds the front end sample and hold block is very important. The speed and accuracy of the converter is highly dependent on the performance of the S/H circuit.
The fastest S/H circuits operate in open loop gain mode [1], [2]. However, their accuracy tends to be limited. Closed loop configuration makes it possible to achieve higher resolution, but the required high gain limits the speed of the circuit.
Fig. 1 shows a basic open loop sample and hold circuit. The gain of this S/H circuit is one which is suitable for front end circuits. The operation of the circuit consists of two phases: the sample phase and the hold phase. In the sample phase the input signal is sampled in the capacitor $C_h$ through the switch $S_1$. In the hold phase the switch is open and the sample is held on the capacitor, and buffered through the buffer B1. According to this discussion the buffer, or the op amp, if closed loop gain is used, is not optimally utilized since it is idle during the sampling period. Double sampling effectively gives a factor of

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two increase in the sampling rate compared to the basic S/H topology while maintaining better utilization of the circuit components which in turn leads to an improved power consumption.

Fig. 2 represents a double-sampled S/H circuit, while the sample is taken in the upper capacitor during the period $\phi$, the lower one is connected in the hold configuration during the period $\bar{\phi}$, and the vise versa. Thus a new sample can be read from the output twice every cloek cycle. The sampling rate is doubled but the double sampling scheme introduces more switches which introduees some unwanted source of errors. Source of errors in the switches and overcoming it will be discussed later.

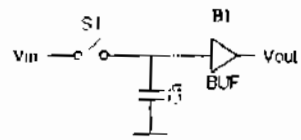



Fig. 1. A basic open loop sample and hold circuit

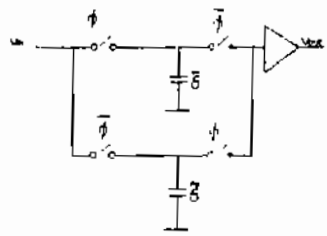


Fig 2. A double sampling S/H circuit

Because the sample and hold circuit presented in this work operates in the current mode, a precise high performance current mirror is needed as an important part of the circuit and will be discussed in the following section

## 2. High performance current mirror circuit

The current mirror is dominant part of the current mode approach, in this work we adopted a circuit presented in [3]. Fig. 3. Shows a conventional MOS current mirror circuit, In this circuit the drain or gate voltage of M1 changes when the ioput signal current $I_{in}$ changes. Voltage change at the input node can be expressed as:

$$\Delta V = \frac{\Delta I_{in}}{g_m} \qquad (1)$$

where gm is the transconductance of M1. This causes the drain to source voltage of M1 to differ from that of M2 as a result a current mismatch between $I_{in}$ and $I_{out}$ is introduced .

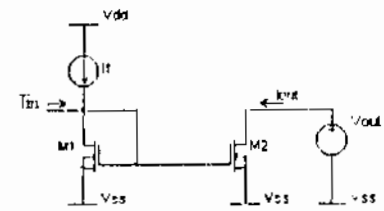



Fig. 3 Conventional MOS current mirror

Similarly when $V_{out}$ changes, $I_{out}$ changes due to the finite output resistance of M2, it can be expressed as:

$$\Delta I_{out} = \frac{\Delta V_{ds}}{r_{ds}} \qquad (2)$$

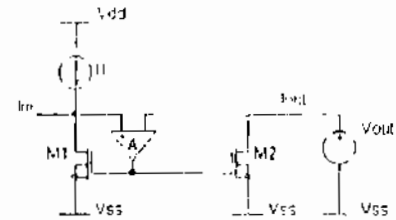



Fig. 4 High accuracy current mirror

Fig. 4. Shows a circuit that can minimize the dependence of the voltage change on the current change at, the input the voltage change is suppressed by the gain of the op-amp and becomes as follows:

$$\Delta I = \frac{\Delta I_{in}}{A \cdot g_m} \qquad (3)$$

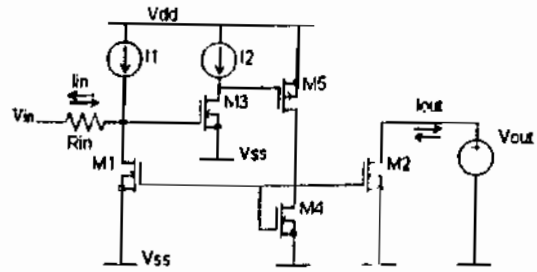



Fig. 5. Realization of the accurate current mirror

Fig. 5 shows the actual realization of the suggested current mirror presented conceptually in fig. 4 Transistors M3 through M5 and the bias current source I2 form the amplifier. Same technique can be done at the output side to enhance the output resistance of the current mirror in order to reduce the change in the output current $I_{out}$ due to the change in the output voltage $V_{out}$. This way an improved current mirror can be achieved. In the following section a description of the design of the S/H circuit will be presented.

## 3. Double sampling S/H circuit Design

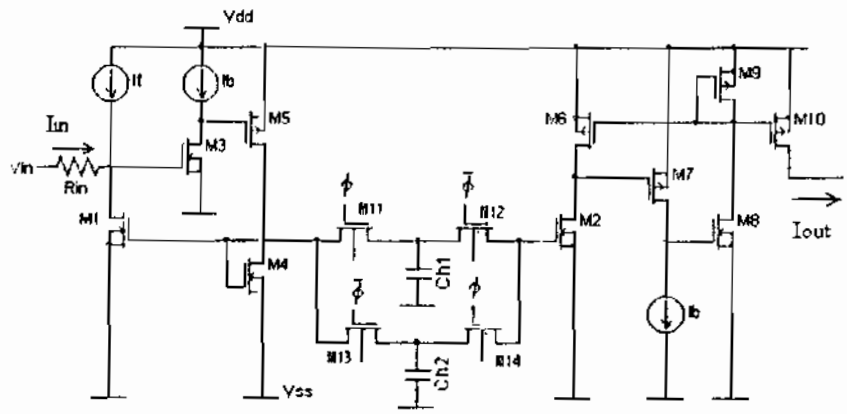



Fig (6) Current mode double sampling S/H circuit

Fig. 6. Represents the design of a double sampling current mode S/H circuit by placing analog switches M11 through M14, derived by the clock phases $\phi$ and $\bar{\phi}$ , and the holding capacitors $C_{h1}$, $C_{h2}$ . At the clock period $\phi$ transistor S1 turns on allowing the capacitor $C_{h1}$ to sample signal and allowing $C_{h2}$ to be in hold mode. At the clock period $\bar{\phi}$, $C_{h1}$ becomes in hold mode and $C_{h2}$ in sample mode. As a result the drain source current of M10 or $I_{out}$ is the sampled $I_{in}$ plus the constant current I1. Transistor M6 through M10 are the PMOS based version of the circuit in fig. 5 required for enhancing the output impedance of the current mirror for accurate current ratio. The analog switches adds unwanted source of errors, in order to reduce the switches feed through errors The complete sample and hold circuit is implemented in a fully differential configuration as shown in Fig 7, where two symmetrical circuits similar to the circuit of fig 6 is connected to the input of a differential amplifier The first circuit passes current equal to $I1-I_{in}+\Delta I$ to the differential amplifier where the second circuit passes current equal to $I1+\Delta I$, where $\Delta I$ is the error current due to the switches feed though The output of the differential amplifier cancels the error

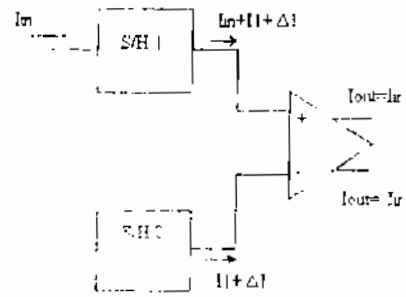
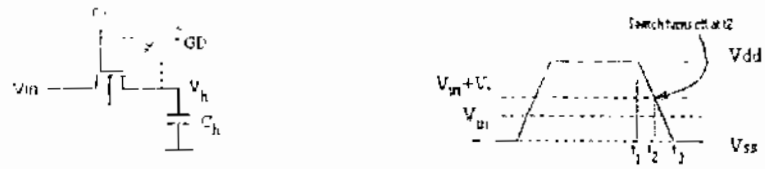



Fig 7. Differential Sample and Hold Configuration




(a) (b)

Fig. 8 Switch feed through effect in MOS switch
(a) Switch, (b)Gate voltage waveform

Also the figure shows that the error due to switches feed through cancel each other, however, means for reducing switches feed through errors needs to be addressed.

## 4. Sources for sampling error

One of the most serious factors affecting the performance of the high precision CMOS sample-and-hold circuits is charge injection due to clock feed through [4]. Fig. 8 shows the effect of the charge injection an N MOS switch, when the clock signal goes from Vdd to Vss the switch turns off at $t_2$. From $t_2$ to $t_3$ the switch is off and charge is injected into the S/H capacitor $C_h$ from $C_{GD}$ ( the parasitic capacitor between the gate and the drain of the switch). As a result, the voltage across the capacitor is decreased. This introduces a pedestal error $\delta V_h$ which can be expressed as:

$$\delta V_H = \frac{C_{GD}}{C_H + C_{GD}}(V_{in} + V_t - V_{ss}) \qquad (4)$$

where $V_t$ is the transistor's threshold voltage, $C_h$ is the hold capacitor, $C_{GD}$ is the parasitic capacitor between the gate and drain.

It can be seen from (4) that the feed-through results in an offset which is a serious problem in high precision sample and hold circuits. Several methods have been proposed to overcome this problem. These includes charge cancellation by adding dummy MOS transistors, offset voltage cancellation by adding a network [4], and by using miller hold capacitance [5], and by minimizing the dependence of the feed through error on the input signal [6]. However, charge cancellation methods are sensitive to device parameters. It is worth mentioning that reducing the size of the switch transistor leads to a small $C_{gd}$ which result in reduction of the feed through error as seen in equation (2). In this paper, the differential configuration is used to cancel the switch feed through.

Other source of error is the on resistance of the MOS switch. In CMOS technology the switch can be implemented with a single NMOS or a single PMOS transistor. The NMOS switch offers low on-resistance when operated near the negative supply voltage but the closer the input signal to the positive supply voltage the less conductive the switch becomes eventually it is cut off one threshold voltage below the supply. The operation of the PMOS is just the opposite A CMOS switch or transmission gate may be used. it offers a finite on resistance in the whole voltage range between the supplies. Another possibility to achieve the same is to control the single transistor switch with a gate voltage greater in magnitude than the supply voltage, thus a voltage boosting circuit is required.

## 5. Simulation Results

The designed circuit is simulated using Spice in 0.5 um CMOS using BSIM3v3.1 Device parameters. Fig 8 shows the functional simulation of the double sampling current mode S/H circuit. The switches used are NMOS transistor with of W=10um L=1um,and aspect ratio=W/L=10, $C_{h1}$=$C_{h2}$=0.3pf The input current was varied from –200uA to +200uA, the supply voltage is 3V, while the gate voltage is boosted to

5V. The output is plotted as shown in Fig. 9. The current error is calculated at different sample steps and plotted as shown in fig 9, the figure displays the maximum of .48uA of error current for the various sample steps included in the rising edge of the input, and 0.45 uA in the falling edge. The effect of the clock feed through is almost completely eliminated. The error signal becomes the half bit equivalent error for 10-bit accuracy The circuit is found to dissipate 10mw, the folded cascode configuration makes the circuit suitable for low voltage applications.

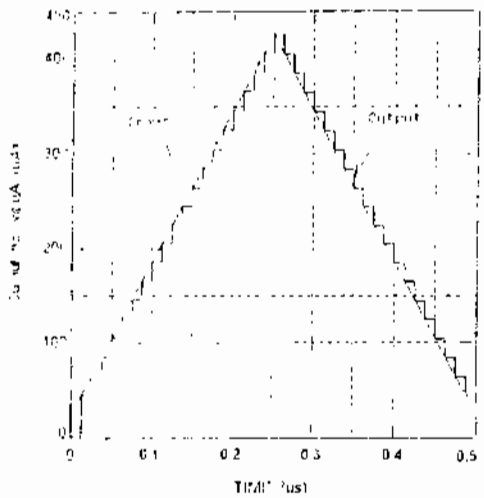



Fig 9 Functional simulation of the S/H circuit

Fig 10 Current Error at different sample steps

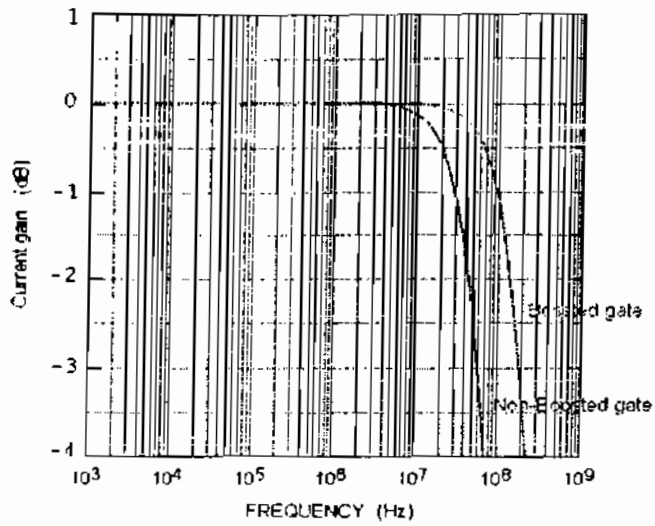



Fig. 11. Frequency response of the S/H

Fig 11simulates the frequency response of the sample and hold circuit where the input current signal was 200uA peak to peak, the figure shows a 3db frequency bandwidth of 200 MHz for the circuit with boosted gate voltage, while that for the circuit with non boosted gate voltage is 60MHz

## 6. Conclusion

Simulation results represent that a double sample S/H circuit with 40 MHz clock, has a double sampling rate of 80 Ms/s Results also shows error current suitable for 10-bit accuracy

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