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# Development of a Microcontroller-Based PWM DC to a Dual-Stage Thyristor Full Bridge Inverter.

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# DEVELOPMENT OF A MICROCONTROLLER-BASED PWM DC TO A DUAL-STAGE THYRISTOR FULL BRIDGE INVERTER

بناء عاكس ثايوستور قنطره كامله مغذى من تيار مستمر معدل النبضه بالستخدام متحكمات دقيقه

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فى هذا البحث يتم انشاء عاكس قنطره كامله بطريقه مقترحه. هذا العاكس يتميز عن العاكس التقليدى بانه ذو كفاءه عاليه و مفاقيد اقل كما ان عمليه اشعال مفاتيحه الالكترونيه تتم باستخدام المتحكمات الذكيه. و قد تم اضافه مفتاح الكترونى (ترانزيستور) يوصل على التوالى مع قنطره العاكس يعمل كمقطع تيار. و يعمل هذا المفتاح الالكترونى المقترح على انشاء تتابع نبضى جيبى خلال فتره زمنيه تساوى زمن الدوره الكامله لتردد الحمل. و يعمل المفتاح المقترح ايضا على الاستغناء عن دوائر الاخماد المعقده و التى تستخدم مع الثايرستورز.

**Abstract**

In conventional pulse width modulated full bridge inverters; all power devices are switched at high frequency and are consequently subject to significant power losses. In this paper, the bridge switches are controlled at the low frequency of the load voltage. The proposed inverter is shown to have smaller device losses and higher power transfer efficiency than commonly used control schemes, while producing a lower harmonic distortion in the ac output voltage. The proposed system is microcontroller-based trigger system which provides the pulse train to the IGBT buck converter switches and the main switches of the bridge inverter, the microcontroller is programmed to provide a sinusoidal pulse width modulated signal in a corresponding matter to the conventional system but it works at high efficiency, precision and with low components. The proposed dual-stage system can eliminates the commutation circuit since when the IGBT buck is off the current through the main switch thyristors reduced to zero.

## Introduction

DC to AC inverters are widely used in motor drives, uninterruptible power supplies and photovoltaic-utility grid interface or stand-alone PV system. The full bridge inverter configuration shown in Figure 1 using thyristors or switches, $T_{M1}$, $T_{M2}$, $T_{M3}$, and $T_{M4}$ are controlled by a variety of Pulse Width Modulation (PWM) techniques. As the switching frequency is increased, a high quality output voltage waveform can be more easily recovered by low-pass filtering [1]. During a typical turn-on or turn-off operation, the voltage across load remains constant near to the dc bus voltage for a significant portion of the switching transient, while a relatively large current is being commutated. Consequently, the inverter objected to high power losses which increase linearly with the switching frequency. This not only impacts the power transfer efficiency of the inverter, but also increases the size and cost of heat sinks required for effectively radiating heat loss to avoid inverter failure [2]. The application of dual-stage has been developed for the MOSFET or IGBT full bridge inverter as a multilevel converter [3]. In this paper a new method introduced to the thyristor-based full bridge inverter by using the dual-stage technique to reduce the switching losses during the PWM scheme. This method can be used also to eliminate the commutation circuits. In reality the commutation will not be varnished but it will be used as the so called auxiliary soft-switches [4]. These circuits perform a zero current transition of the inverter and are applied

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for the high power ac motor drive applications to commutate the current during the transition [5]. In the dc to ac inverter presented in this paper, the bridge switches are commutated at the output frequency ($f_1$), while the high-frequency pulse width modulation ($f_{carrier}$) is handled by using the microcontroller as programable triggering circuits [6]. The proposed control scheme is used to trigger the overall thyristors and in the same time providing PWM scheme to the IGBT buck converter by using the programmed intelligent controller (PIC) [7], for retaining the sine output waveform from the inverter, a low pass filter is designed for this purpose. Figure 1 show the topology of the proposed dual stage thyristor full bridge inverter with IGBT($Q_1$) as the switch which will perform the PWM of the DC voltage.

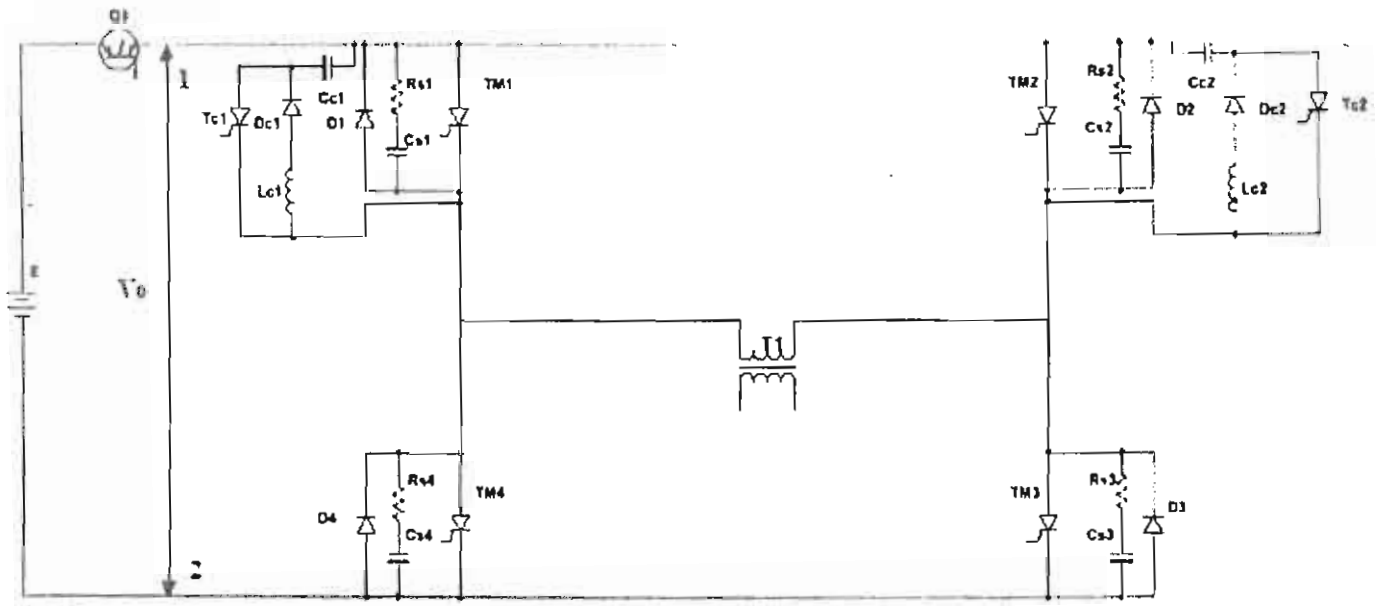



Figure 1- Dual-stage PWM full- Bridge Inverter

**Sequence of Operation of the Dual-Stage Inverter**

The pair of thyristors and the IGBT must be triggered simultaneously throughout the half cycles as follows:

1-Thyristors TM1 and TM3 are triggered together from the same triggering pulse of the IGBT-Q1 buck converter during the positive half.

2- Thyristor TC1 is triggered t just before the end of positive half cycle of the output wave form to commutate $T_{M1}$ and $T_{M3}$. $T_{C1}$ is naturally commutated at the end of the commutation cycle of the two thyristor.

3- Thyristors $T_{M2}$ and $T_{M4}$ are triggered together from the triggering pulse signal of the IGBT-Q1 buck converter during the negative half.

4-Thyristor TC2 is triggered just before the end of the negative half cycle to commutate TM2 and TM4, and then it will be naturally commutated at the end of the commutation cycle of the two thyristors.

The timing diagram of the dual-stage inverter and the commutation circuit will be explained later. The commutation process is accomplished by using the technique of resonant impulse. When thyristors TM1 and TM3 are in on-state, the current will pass from the source through IGBT buck converter,

$T_{M1}$ and $T_{M3}$ to the load, frequently, as thyristors TM2 and TM4 are in on-state, the current will pass from the source through IGBT buck converter, $T_{M2}$ and $T_{M4}$ to the load. Figure 2 shows the topology of the dual-stage inverter with its commutation circuits. As the triggering signal is applied to the first which branch including the thyristors $T_{M1}$ and $T_{M3}$, the current passes through IGBT-Q1 buck converter, $T_{M1}$, load (primary side of transformer) and $T_{M3}$ as shown in figure 2.

**Sinusoidal Pulse modulation by dual-stage inverter**

The output voltage waveform for sinusoidal-pulse duration modulation is illustrated in Figure 4a [8]. In this Figure, the duration of each pulse changed sinusoidally according to its position in the sinusoidal waveform. Figure 4b represents how to determine the duration of each pulse. The turning on and off of the switches are executed by a flexible microcontroller circuit.

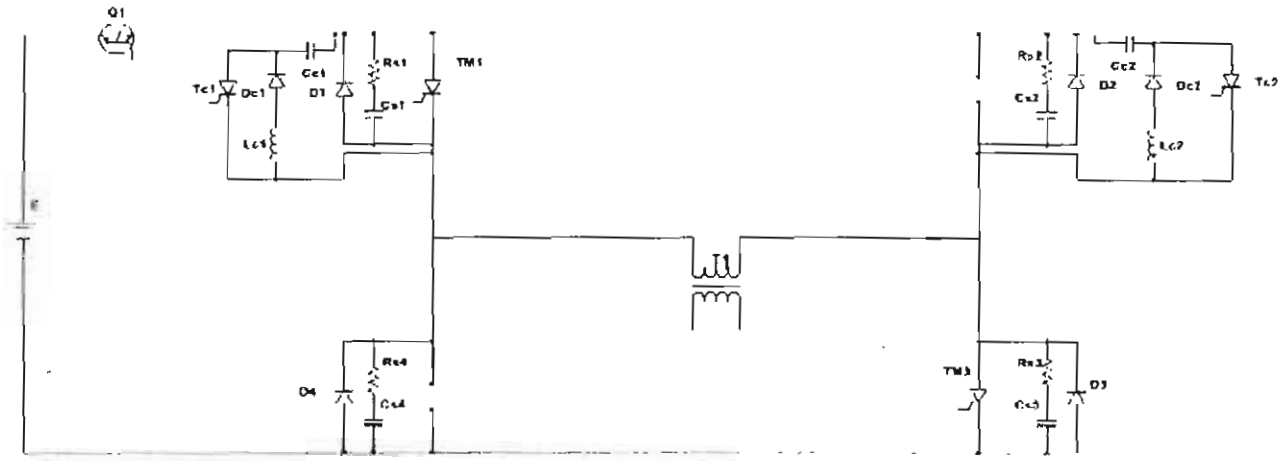


Figure 2 -The equivalent circuit of the inverter for the first half cycle of the operation

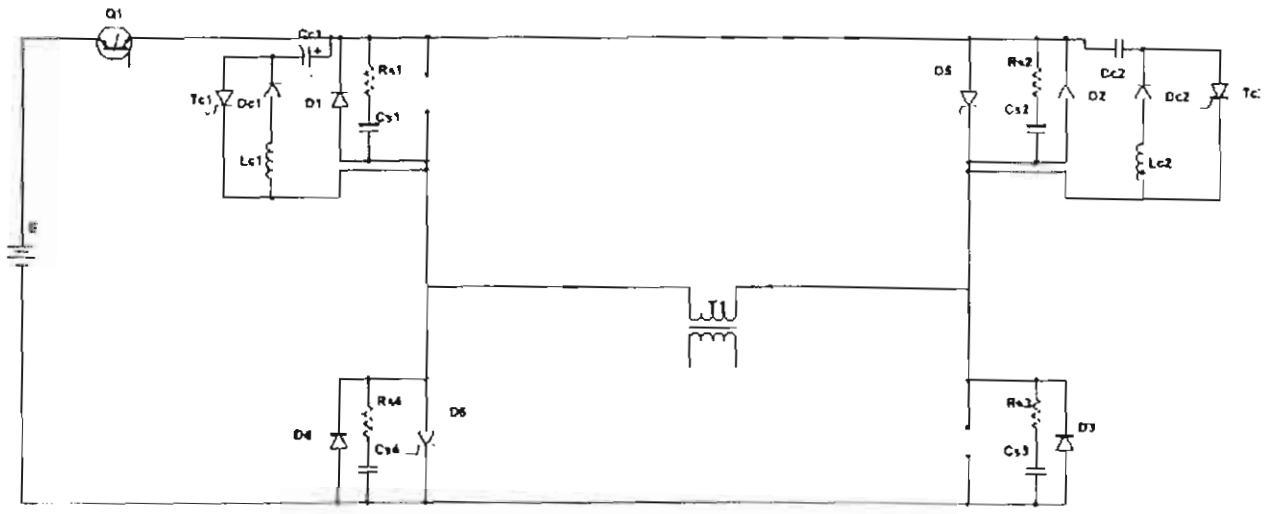
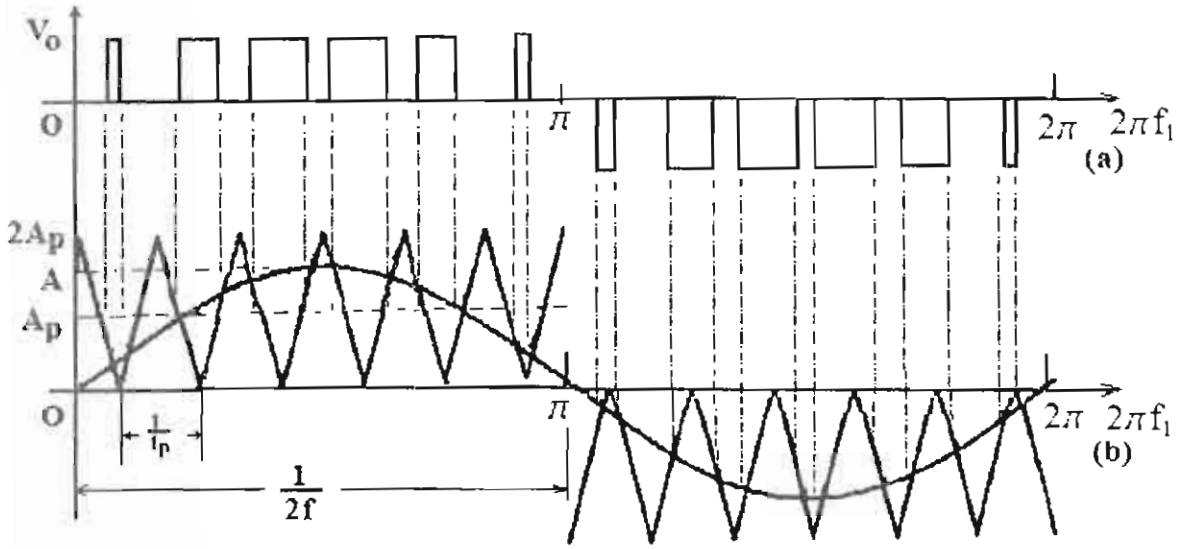


Figure 3 - The equivalent circuit of the inverter for the second half cycle of the operation




Figures 4-Output waveform with sinusoidal-pulse modulation

The control function consists of a train of signals sinusoidally variable pulse width generated by the microcontroller. The duration of each pulse applied to the IGBT-Q1 buck converter is given by [1]:

$$d(t)=m_o 6 \sin 2\rfloor f_1 t 6 \qquad (1)$$

Where:

d(t) is the time-varying duty ratio and $m_o$ is the modulation index which is selected in the range of $0<m_o<1$, and $f_1$ is the desired frequency of the inverter.

**Analysis of the Operation of dual-stage inverter**

The dual inverter switches are triggered by using sinusoidal pulse width modulated signals output from the programmable intelligent microcontroller (PIC). The operation is then converted to suitable code to the PIC memory. The pulse width modulation scheme (PWM) is used to control the IGBT-Q1 buck converter. The average voltage across terminal 1-2 in Figure 1 given by

$$V_{12} = d(t)V_B \qquad (2)$$

Where:

$V_B$ is DC. Input voltage to the dual-stage inverter. If the duty ratio d(t) is made to vary slowly with respect to the switching frequency of Q1, the loeal average value of the buck converter voltage is given by:

$$\bar{V}_{12} = \bar{d}(t)V_B \qquad (3)$$

The buck converter IGBT-Q1 operates as a DC chopper according to the time varying modulation pulses d(t). the output of the pulse width modulator is shown in Figure 4a. The corresponding pulsc triggering signal is used as thc gate control signal for the IGBT and the corresponding thyristors in the same time. The instantaneous value of thc voltage output across the load is given by;

$$V_o = \begin{cases} + d(t)VB & TM1, TM3\ ON \\ - d(t)VB & TM2, TM4\ ON \end{cases} \qquad (4)$$

The control functions of the above operation can be packaged into a suitable code to be downloaded into the PIC EEPROM to drive the dual-stage inverter as following:

1. Create a sine wave with the frequency equal to the desired inverter frequeney ($f_1$=50) and variable amplitude A

$$c(t) = A \sin(2\pi f_1 t) \quad (5)$$

2. Set the amplitude ($A_p$) of the modulating signal (triangle wave) such that $2A_p > A$.
3. Set the frequency ($f_p = f_{carrier}$) of the modulating signal equal to the IGBT switching frequency.
4. Define the period of the modulating signal as;

$$T_p = \frac{1}{f_p} \quad (6)$$

Where: $T_p$ is the period of the modulating signal.

5. The instantaneous of the modulating signal is given by ;

$$m(t) = 2A_p\left[\left(\frac{t}{T_p}\right) - floor\left(\frac{t}{T_p}\right) - A_p\right] \quad (7)$$

Where: m(t) is the function representing the modulating triangle signal.

The generation of the PWM waveform will depend on the triangular and instantaneous amplitude of the sine wave.

6. The comparison between the instantaneous value of the triangle and sine waves is given by;

$$S(t) = \begin{cases} E \text{ at } m(t) > c(t) \\ 0 \text{ at } m(t) < c(t) \end{cases} \quad (8)$$

Where E is the output voltage of the PIC pins (approx. 5V)

The number of pulses generated during a half cycle of the output waveform is;

$$N = \frac{f_p}{2f} = \text{integer} \quad (9)$$

Turn-on and turn-off angles of the IGBT-Q1 buck converter are determined according to equation 9. The output voltage is controlled by varying the amplitude A over a range $0 \le A \le A_{max}$, where $A_{max} > 2A_p$. if $A_{max}$ is made very large, within the limit, output voltage $V_o$ approaches to the rectangular waveform. The determination of the harmonic amplitudes is relatively complicated, however, it is found that for $0 \le A/A_p \le 2$ all harmonics of order $n<2N$ are eliminated. For $A/A_p>2$, low-order harmonics appear [8, 9]. Since pulse-width is no longer a sinusoidal function of the angular position of the pulse. For the PWM technique, the frequency harmonics are in the area of the switching frequency. The content of the harmonic is determined according to the frequency of the triangular carrier wave m. The harmonic frequencies $f_n$ are given by [1]

$$f_n = \left(j\frac{f_{tri}}{f_1} \pm k\right) f_{tri} \quad (11)$$

j, k are always odd.

**Performance of the Proposed Dual -PWM Full Bridge Inverter**

The performance of the proposed dual inverter designed is compared with conventional triggering inverters as they loaded with similar load. The two cases containing similar switches and DC supply as shown in Table 1.

The ratio of $f_{carrier}/f_1$ ($f_{carrier}$ is the frequency of the triangular wave form) must be an odd and integer. This is because the dual PWM inverter must sustain odd quarter wave symmetry at its output. This lead to the elimination of all even harmonics. The selection of the frequency of the dual switch is chosen very greater than the output frequency of the inverter. Hence more harmonic will be eliminated. Since, the harmonic frequencies occur around twice the carrier frequency.

Table 1 the components specification of the proposed dual inverter.

| The specification of the inverter | The corresponding value |
|---|---|
| Load | 2.5 A |
| Frequency of output voltage, $f_1$ | 50 Hz |
| Switching frequency, $f_p$ | 150 Hz (for the IGBT PWM circuit) |
| DC supply voltage, E | 60 V |
| Main switches, TM1, TM2, TM3, and TM4 | Thryistors ( BT151) |
| PWM switches, $Q_1$ | IGBT, GT60M101 |
| Output filter type | 2nd order Butterworth, Pass Band 0-1kHz |

The harmonic distortion degree of the output voltage waveform is [10]:

$$\%THD = 100\frac{V_{dis}}{V_{rms1}} = 100\frac{\sqrt{V_{rms}^2 - V_{rms1}^2}}{V_{rms1}} \quad (12)$$

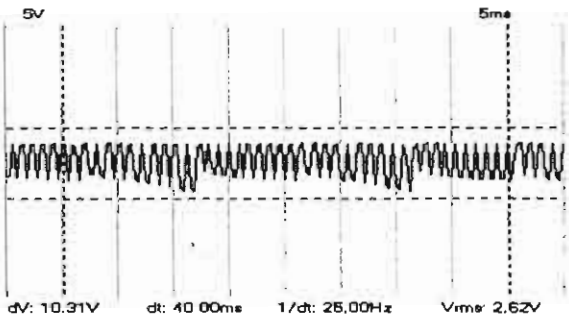
Where;
$V_{dis}$ =RMS voltage distortion [V]
$V_{rms1}$ =fundamental frequency RMS voltage [V]
$V_{rms}$= RMS voltage [V]
THD =Total harmonic distortion [V]

Table 2, comparison between dual PWM and PWM modulated inverter

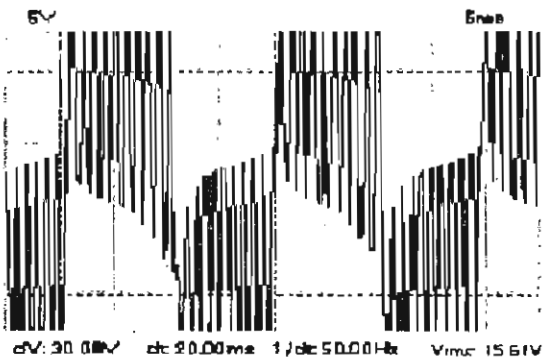
| Parameter | Dual-stage PWM inverter | Normal inverter |
|---|---|---|
| Total Harmonic Distortion (THD) | 1.02 | 1.4 |
| Power loss from $Q_1$ | 15-2.4%(500w) | Not used |
| Combined power (TM1,TM2, TM3, and TM4) | 13-2.6%(500w) | 40w-8% (500w) |
| Power Transferred efficiency | 95% | 92% |

**Inverter waveforms**

The pulse widths vary sinusoidally, as expected from the theoretical waveform shown in Figure 5. The waveform for the buck converter output voltage for the proposed circuit is shown in Figure 6. Figure 6 also shows the unfiltered output voltage for the proposed inverter for two schemes of operation; the first is the output of the inverter without the proposed dual-stage PWM buck converter, the second with the proposed PWM buck converter. The corresponding frequency spectra for the unfiltered output voltages under the above two scheme of operation of the inverter are shown in Figures 6(b), and 6(d), respectively. In the first two cases the significant harmonics occur around the switching frequency. However the inverter without PWM has higher harmonic content.

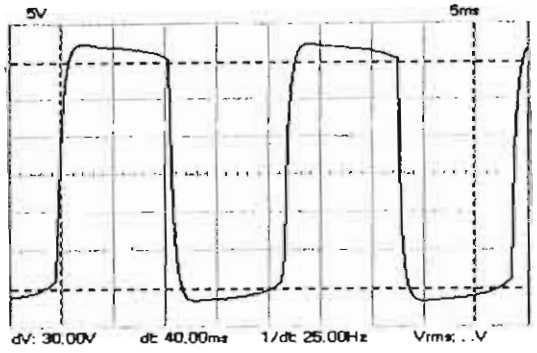



(a)

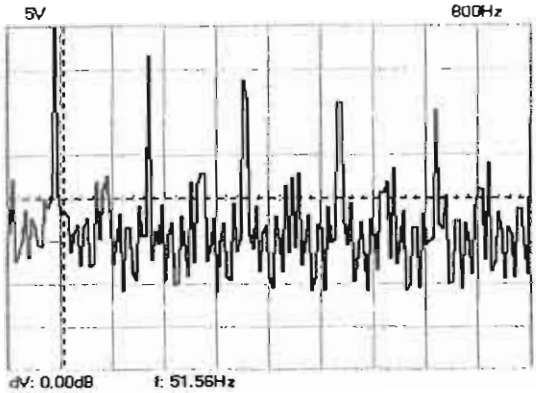



(b)

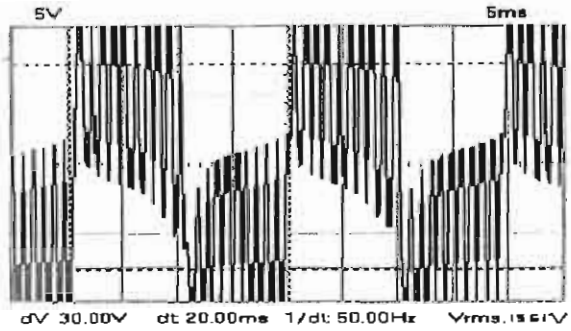
Figure 5: (a) Buck Converter Output Voltage, (b) Unfiltered Output Voltage of Proposed Inverter.



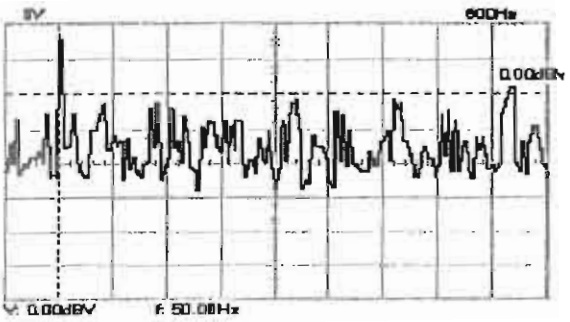

(a)




(b)




(c)




(d)

Figure 6 (a) The output voltage of the inverter without PWM, (b) Power Spectrum of Unfiltered Load Voltage, (c) The output voltage of the inverter with dual-stage PWM, (d) Power Spectrum of Unfiltered Load Voltage

**Adaptive Filter of inverter output voltage**

For obtaining a sinusoidal ac output voltage, the low-pass filter formed by L and C in Figure 7 extracts the fundamental component of $V_{AB}$. Hence the load voltage, $V_0$, is effectively the local average value of $V_{AB}$ ($V_{AB}$ is $V_{12}$), as shown in Figure 8.

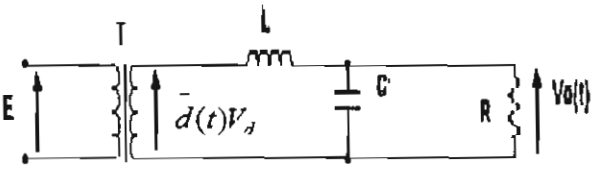



Figure 7: Averaged Circuit Model for Proposed Dc to Ac Inverter

The harmonic appears of the dual-stage PWM inverter at higher frequency, compared to Those of the inverter without dual stage PWM. The filtered load voltages for the dual-stage PWM inverters are shown in Figures 8. The proposed dual-stage PWM inverter is seen to produce the lower value of total harmonic distortion in the load voltage, as shown in Table 2.

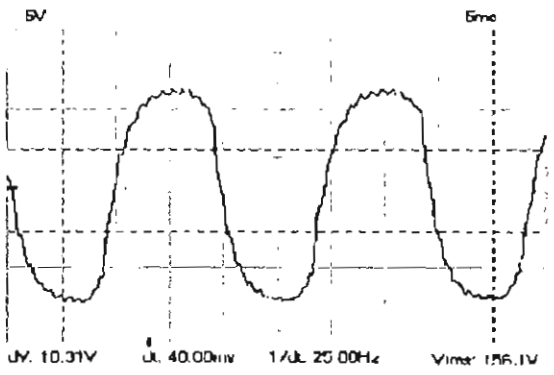



Figure 8 the output of the filtered output voltage

## CONCLUSION

This paper has presented a new method for the operation of the full bridge thyristor-based inverter with reducing the overall switching power loss and improving the quality of the output voltage waveform in a dc to ac pulse width modulated inverter. It has been shown that the proposed circuit and control strategy which achieved with a high accuracy pulse triggering microcontroller-based circuit to produce low-distortion output voltage waveforms, while improving the power transfer efficiency over conventional schemes. The proposed scheme is triggered by using programmable intelligent controller (PIC-Microcontroller). This method provides more flexibility , high precision as well as high synchronization switching between the buck converter and the inverter main switches.

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# SENSORLESS DIGITAL CONTROLLER FOR SWITCHED RELUCTANCE MOTOR

# المحكم الرقمي بدون مجس لمحرك المعاوقة الانتقالي

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في الأونة الأخيرة- خاصة في التطبيقات الصناعية – زادت الحاجة لاستخدام محركات المعاوقة الانتقالية. لذا تم في هذا البحث دراسة و تصميم و بناء دائرة محكم رقمي لمحرك المعاوقة الانتقالي بدون حساسات. و يقدم هذا المحكم كثير من المزايا منها بساطة التركيب و سهولة البناء و رخص التكاليف. كما أن هذا المحكم يمكنه التعامل مع المحرك في كل من نظامي التحكم (المفتوح و المغلق) للوصول بالنظام إلى أداء أكثر استقرارا و أوسع نطاقا في التشغيل.

تم تسجيل نتائج تشغيل محرك المعاوقة الانتقالي عند ترددات من ٦,٧٥ ذ/ث إلى ٢٥ ذ/ث و وجد استقرار كامل للنظام خلال هذا المدى من الترددات و عند حمل مناسب.

## Abstract

Recently, a great interest has been directed to switched reluctance motor and its wide applications in industry; such as: robotics, textiles, servo-drives, domestic drives and electric vehicles. The earliest control techniques used for SRMs were difficult and complicated due to their requirements for a rotor position sensor. The rotor position sensor is a significant contribution to the cost and complexity, and tends to reduce the reliability of the drive system.

In this paper, a simplified sensorless digital controller has been designed, analysised, implemented and tested with SRM of 6/4 pole and 1.1 kW rated power. Moreover, a digital simulation of the SRM supplied from this controller has been developed using MATLAB/SIMULINK program. Some interested measured results have been introduced to illustrate the performance characteristics of the system. Finally, both practical measured results and theoretically calculated results were compared and found much close to each other.

## 1- Introduction

Switched reluctance motors (SRMs) have undergone rapid development in many applications over the last two decades. This is mainly due to the various advantages of SRMs over other electric motors such as simple and robust construction, and fault-tolerant performance [1]. From the construction point of view, it is the simplest of all electrical machines. Switched reluctance motors are mainly doubly salient magnetic structure, built up from a stack of steel laminations. The stator phase winding comprises a set of coils, each of which is usually wound around a pair of opposite pole [2]. The rotor contains no conductors or permanent magnets. The operation principles and control are explained in details in [3,4]. The drawbacks often cited for the SRM; that they are difficult to control, require a shaft position sensor to operate, tend to be noisy, and they have more torque ripple than other types of motors. The torque ripple problem attracted researchers to solve it references [1,5-10] explore many methods to solve this problem.

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Recently, sensorless operation is available and the improvements in digital and power electronics solve the control problem. Numerous literature discuss this issue [11-15].

The waveform detection technique, which uses the current chop rise time in the active phase for monitoring rotor position is presented in [11]. Measuring the mutually induced voltage in an inactive phase, which is either adjacent or opposite to the energized phase of an SRM is used in [12]. A PWM voltage control method has been introduced in [13]. High-resolution sensorless position estimation, using either flux-linkage or current to correct for errors in rotor position is presented in [14]. Another method has been described in [15], based on a stored flux-linkage / current / position characteristics.

This paper introduces a new simple low-cost sensorless controller. This controller has been tested on 6/4 SRM of 1.1 kW rated power. To verify the controller output, a mathematical model of SRM has been developed using MATLAB \SIMULINK software. First, the SRM mathematical model, the driving circuit implementation and finally the simulation results are presented.

## 2- SRM Mathematical Model

Dynamic analysis comprises the set of the electrical differential equations of motor phases and mechanical differential equations, are solved simultaneously (for appropriate switching conditions) to calculate the torque and current waveforms. The instantaneous voltage equation across the terminal of a phase winding can be expressed by Faraday's law as:

$$V_{dc} = R_{ph}\, i + \frac{d\psi}{dt} \qquad (1$$

Where;

$V_{dc}$ := D.C terminal voltage
$R_{ph}$ := Phase winding resistance
$i$ := Phase current
$\psi$ := Phase flux-linkage

Due to the nature of this motor, saliency and the effect of the magnetic saturation, the flux-linkage varies as a nonlinear function of rotor position and the phase current. So equation (1) can be rewritten as follows:

$$\frac{d\psi_n(\theta, i_n)}{dt} = V_{dc}|_n - R_{ph}\, i_n \qquad (2$$

Where; n:= varying from 1 to q
q:= number of phases
the mechanical equations of SRM

$$\frac{d\theta}{dt} = \omega \qquad (3$$

$$\frac{d\omega}{dt} = \frac{1}{J}\left[\sum_{n=1}^{q} T(\theta, i_n) - T_L\right] \qquad (4$$

To solve these equations (2), (3), and (4) in this form to obtain waveforms of phase currents and torque against time (rotor angle), it is required to define the magnetic behavior of the SRM in the form of look-up tables $i(\theta,\psi)$ and $T(\theta, i)$ to enable the values of current and torque of each phase to be updated after each step of integration, which are inserted into right-hand side of the foregoing equations. Both tables $i(\theta,\psi)$ and $T(\theta, i)$ are derived from the input table $\psi(\theta, i)$. The table $i(\theta,\psi)$ can be obtained by numerical inverse of the input table $\psi(\theta, i)$. Also the table $T(\theta, i)$ can be obtained by numerical differentiation using:

$$T(\theta, i) = \frac{\partial W^{\backslash}(\theta, i)}{\partial \theta} \qquad (5$$

And the table $W^{\backslash}(\theta, i)$ can be obtained by numerical integration using:

$$W^{\backslash}(\theta, i) = \int_0^i \psi(\theta, i)\, di \qquad (6$$

## 3- Driving Circuit

The proposed digital controller circuit consists of four main stages, as shown in

Figure (1), to generate the required gating signals. These stages are:

1. clock pulse generator or voltage-to-frequency converter
2. special purpose counter
3. digital controller
4. signal interfacing and latching

Which can be shortly explained as follows:
To generate clock pulses a timer device such as 555 integrated circuit is arranged in a circuit of IC555 so as to trigger itself repeatedly. This is applied for open loop control, if we desire the closed loop control another arrangement can be done in order to get voltage-to-frequency converter. This converter works as a tachometer. Its output is a pulse train at a frequency precisely proportional to the applied input. However, using the clock pulse generator or the voltage-to-frequency converter the output of both is a pulse train. These pulses are the input to a binary counter. This counter generates four output signals as shown in Figure (2). This counter can be called a special purpose counter, that generates three output signals and the fourth used to reset it. Now, the digital controller will use the counter outputs to generate three group pulses. These pulses are used to initialize mosfet gates. These signals cannot be directly connected to the electronic power switches for two reasons. The first is the power level of these signals is not sufficient to drive a power switch. The second, and much important reason, is that the power switches are located at different volt levels and they have no common connection. For these reasons, gate drive circuits are essentially required, to raise the power level of these switching signals and isolate the control and power circuit [16]. Six opto-couplers are used for all; current amplifier, isolation and interfacing.

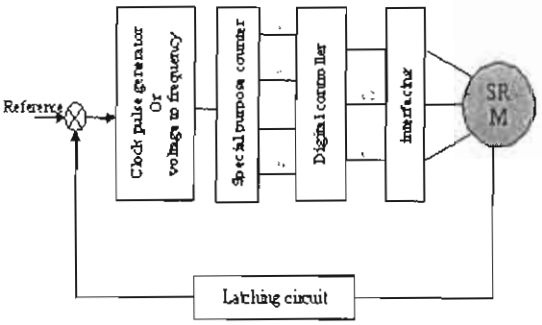


Fig.(1): Sensorless digital controller block diagram.

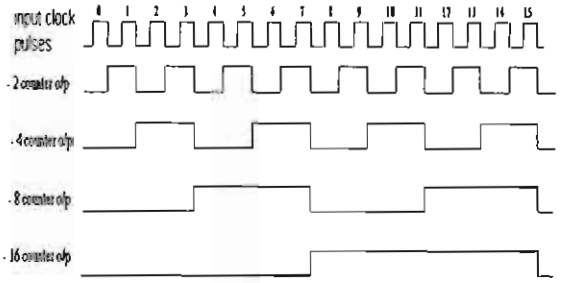


Fig. (2): Input and output of the counter

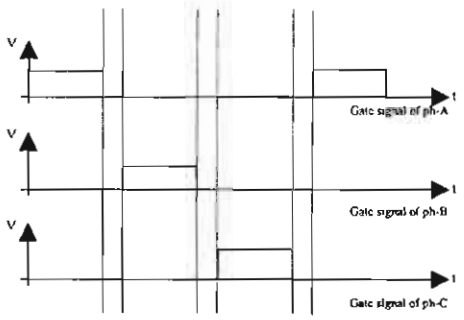


Fig. (3): The gate pulses of the different phases

Figure (4) shows the input and the output signals of the counter in the lab. Figures (5), (6), and (7) give samples of the gating signals at different frequencies.

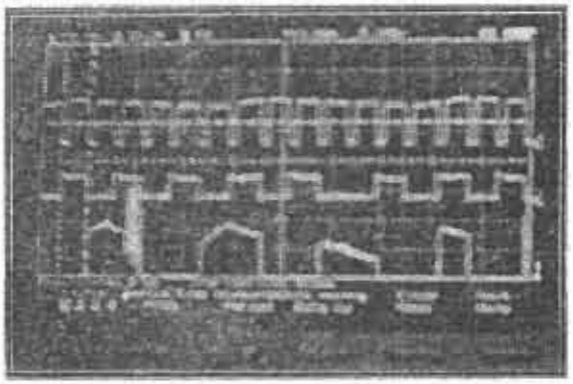

Fig.(4): Counter input and output signals
Ch.1 5 volt, f= 188 Hz, clock pulse input.
Ch.2 5 volt, f= 94 Hz, counter output (divided by 2).
Ch.3 5 volt, f= 47 Hz, counter output (divided by 4).

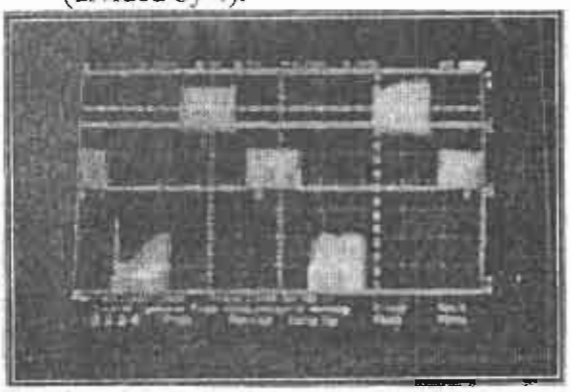

Fig.(5): Three phase gating signals with operating frequency 6.75 Hz
Ch.1 phase A gate signal.
Ch.2 phase B gate signal
Ch.3 phase C gate signal

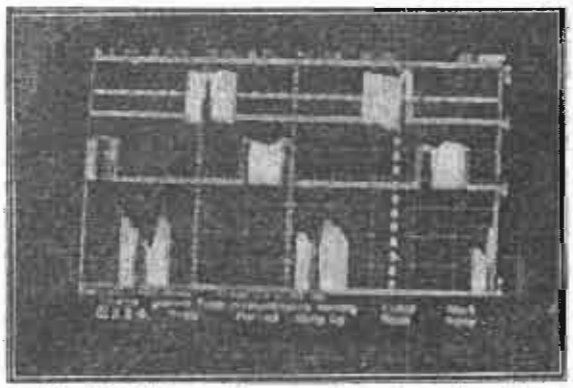

Fig.(6): Three phase gating signals with operating frequency 12.5 Hz
Ch.1 phase A gate signal.
Ch.2 phase B gate signal
Ch.3 phase C gate signal

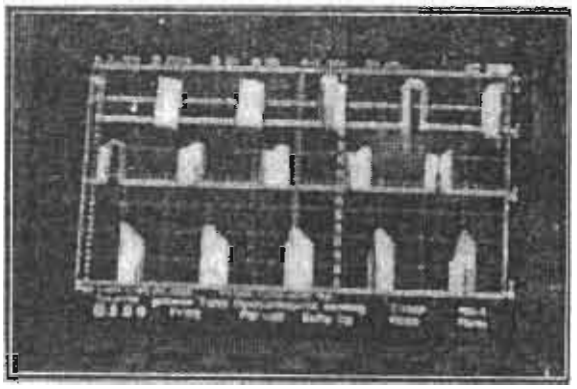

Fig.(7): Three phase gating signals with operating frequency 25 Hz
Ch.1 phase A gate signal.
Ch.2 phase B gate signal
Ch.3 phase C gate signal

## 4- Power converter circuit

The power inverter topology is an important issue in SRM control because it largely dictates how the motor can be controlled. Mosfets are used as the main switches in the present application, due to their advantages and their high performance. Figure (8) shows the proposed power converter circuit. Its principle of operation can be summarized as follows;

When the gate signal reaches to switch T1 the current will follow in the phase A then to switch T1' then to the negative side of the D.C. supply. A duration elapsed empty without any signals to enable the stored magnetic energy in the phase A to be discharged. Then the gate signal of the switch T2 reaches so it conducts and the phase B energized then switch T2'. The rest duration appears again till phase B discharge. Finally the signal of switch T3 reaches making it on and the current passes through phase C, then switch T3' allows the current to return to the supply. The rest duration appears again to discharge phase C energy. Again the gate pulse of switch T1 appears and so on.

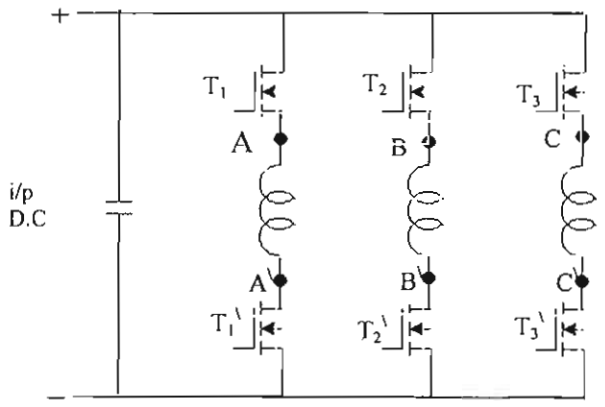


Fig. (8): The power converter circuit

## 5- Simulation results

A mathematical model of SRM is carried out using Matlab/Simulink engine. Here are some results of the simulation model, which verify the controller operation. These results are at the rated speed 750 r.p.m, rated voltage 270 V, switch-on angle –13.5° (the interpolar point), and the switch-off angle at 10°. The gate pulses in Figure (6) present the pulses with frequency equal 12.5 Hz, which corresponds to the rated speed. These pulses are generated from clock pulses of 188 Hz see Figure (4).
The results of the simulation are shown in Figures (9), (10), (11), and (12).

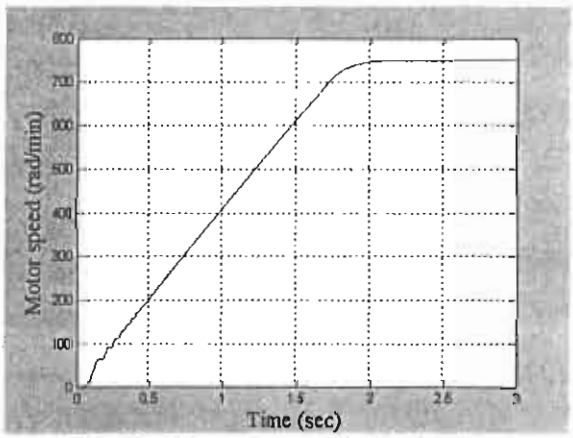


Fig.(9): The motor speed Vs. time.

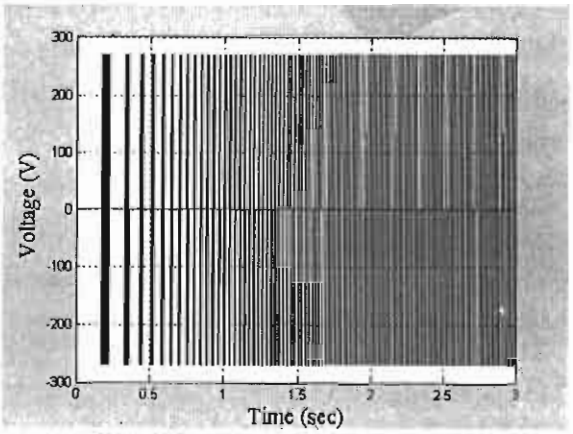


Fig.(10): The DC link voltage

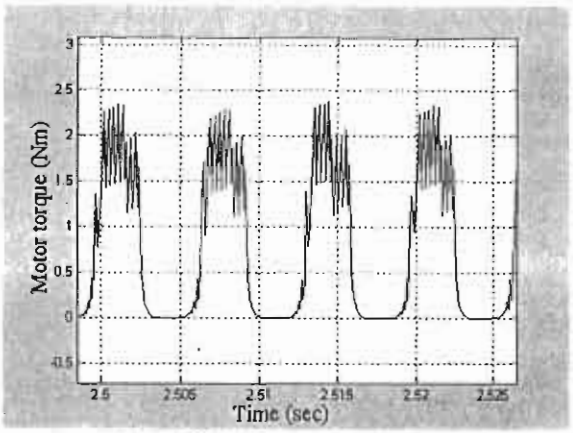


Fig.(11): The motor torque.

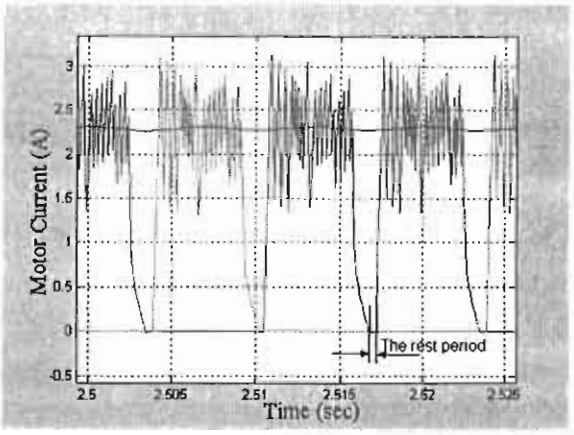


Fig.(12): The motor currents

## 6- Conclusion

A sensorless digital controller of SRM has been designed, implemented and tested. The primary advantages of this controller are simple construction, economical implementation, and can operate in both open loop and closed loop configurations.

Interesting practical measurements and theoretically calculated results have been introduced and they are in agreement.

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