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A Novel XOR Gate Using Single Electron Tunneling Technology.

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A NOVEL XOR GATE USING SINGLE ELECTRON TUNNELING TECHNOLOGY

دائرة جديدة لبوابة (أو الحصرية) بإستخدام تكنولوجيا إختراق الإلكترون الواحد (النانومترية)

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الخلاصة:
إن تكنولوجيا إختراق الإلكترون الواحد (النانومترية) تقدم إمكانية أكبر لتصغير أبعاد المكونات الإلكترونية الحديثة مقارنة بالإمكانيات المتوقعة لتكنولوجيات السيليكون المعروفة (مثل تكنولوجيا معدن-أكسيد-شبه موصل المزدوجة). إن تكنولوجيا إختراق الإلكترون الواحد تعطى القدرة على التحكم فى حركة الإلكترونيات فى الدوائر المصممة. فى هذا البحث سنقوم بإستعراض بعض دوائر الإلكترون الواحد الأساسية فى الأبحاث المنشورة حديثا. وسيتضمن ذلك تفاصيل هذه الدوائر بما فيها قيم المكونات المستخدمة والنتائج المتوقعة لإستخدام هذه الدوائر بإستخدام برنامج المحاكاه على الكمبيوتر (سيمون 2). وفى نهاية البحث سنقدم التصميم الكامل لدائرة إلكترون واحد جديدة تنفذ بوابة أو الحصرية مع نتائج المحاكاه على الكمبيوتر. ويمكن إستخدام نفس التصميم السابق كدائرة جمع نصفية.

Abstract:
Single Electron Tunneling (SET) technology introduces more potential for feature size reduction compared with well-established silicon-based CMOS technology. The SET technology offers the ability to control the motion of individual electrons in the designed circuits. In this paper, some of the basic Single Electron Circuits (SEC) found in the literature is reviewed. The complete schematic diagrams of these basic SEC (inc. parameters for used devices) along with the corresponding simulation results (using SIMON 2.0) of these SEC are included. Finally, a novel XOR SEC, with detailed schematic and simulation results, is presented. The developed XOR SEC can be used as a half-adder SEC.

Keywords:
Single Electron, SET, Single Electron Box (SEB), Single Electron Circuits (SEC), Boolean logic, Linear Threshold Gate (LTG), XOR.

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1. Introduction:

The Single Electron Tunneling (SET) technology is the most promising future technology generations to meet the required increase in density and performance and decrease in power dissipation [1-2]. The main device of the SET circuits is the tunnel junction through which individual electrons can move in a controlled manner [3].

A decade ago, the basic physics of SET was well understood and designing useful Single Electron Circuits (SEC) became the important research area [4-5]. In the past few years, some basic building blocks for SEC had been introduced in the literature [6-9].

In this paper, we first briefly discuss the basic physics of SET in section 2. We review some of the SEC basic building blocks that were introduced in the literature, in Section 3. The full design (inc. detailed schematic diagrams with all parameters for used devices) and simulation results (using the famous Monte Carlo simulator; SIMON 2 [10]) are included. In Section 4, a novel XOR SEC is introduced. The full design and SIMON 2.0 simulation results of the developed XOR SEC are presented. It is worth noting here that the developed XOR SEC can be used as a half-adder SEC. The conclusions are provided in Section 5 followed by the used references in Section 6.

2. The Basic Physics of SET:

The main component of SEC is the tunnel junction that can be implemented using silicon or metal-insulator-metal structures, GaAs quantum dots, etc.

The tunnel junction can be thought of as a leaky capacitor [11]. For very small tunnel junctions (hence, very small capacitance C_j), the movement of only one electron, from one side of the tunnel junction to the other, may produce a noticeable change e/C of the voltage across the tunnel junction. Note that the above $C = C_j + C_e$ where C_e is the equivalent capacitance of the remainder of the circuit, as viewed from the tunnel junction's perspective.

The discreteness of the electrical charge e leads to the Coulomb blockade effect that is widely known in the field of single-electronics. The critical voltage V_c (the voltage needed in order to make one electron tunnel through the junction) is given by [6]:

$$V_c = e/2C \qquad (1)$$

The Coulomb blockade effect is the suppression of electron tunneling across the tunnel junction at voltages $|V| < e/2C$. This means that for such voltages, there will be no increase in the electrostatic energy of the junction capacitor: $CV^2/2$ (in the case of such increase, the energy would be [4]: $C(V \pm e/C)^2/2$.

Today's well-established technologies uses metal junctions with an area about 50×50 nm^2 that lead to a typical capacitance and its corresponding voltage scale (e/C) in the order of 100 aF and 1 mV, respectively.

To avoid the effects of thermal fluctuations on SEC, the thermal energy $k_B T$ should be much less than the typical one-electron charging energy ($eV = e^2/2C$) [4].

$$k_B T << e^2/2C \qquad (2)$$

The above condition limits the practical use of SEC since the working temp. is restricted to be < 1 K. For a room operating temperature (300 K), junction capacitances should decrease to the range of 0.1 aF. To reach this low capacitance level, the size of the devices should go below few nanometers and single electronics enters the areas of atomic physics and chemistry [4].

3. The Basic SEC Building Blocks:

Some of the basic SEC building blocks, found in the literature, are reviewed in this section. The full design (inc. detailed SEC) and SIMON 2 simulation results are also included.

3.1 The Single Electron Box:

The Single Electron Box (SEB) is the simplest device using SET effect. The SEB is composed of one capacitor and one tunnel junction [8].

Fig. 1 shows one possible way of constructing the SEB along with the sawtooth-like output characteristics using SIMON 2. In this configuration of the SEB: with the linear increase of VIN, VOUT increases until it reaches the critical value of $e/2(C_j+C_o)$. Then the tunneling occurs and as a result, the charge goes down and VOUT decreases instantaneously to become $-e/2(C_j+C_o)$. The above process repeats giving rise to the sawtooth-like output.

Fig. 2 shows the other possible way of constructing the SEB along with its output. In this configuration, VOUT increases linearly until the tunneling occurs, then there will be a sudden increase in VOUT due to the charge transfer. The above process repeats giving rise to the linear-step-like output.

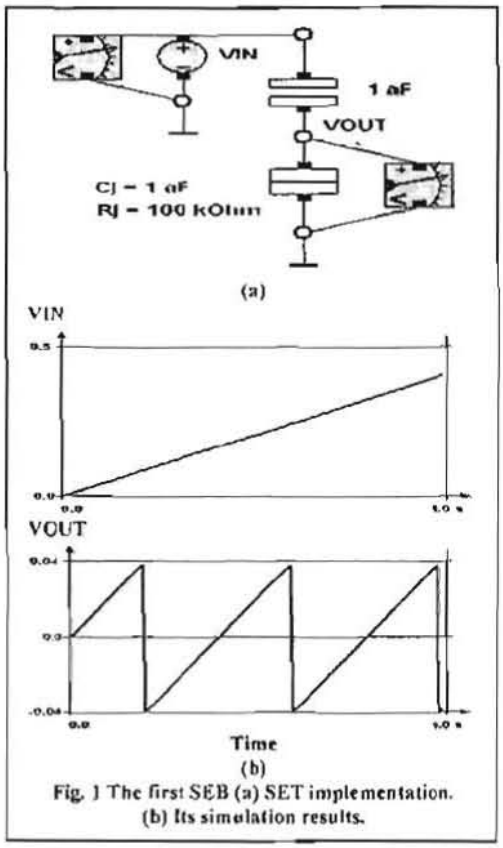


Fig. 1 The first SEB (a) SET implementation. (b) Its simulation results.

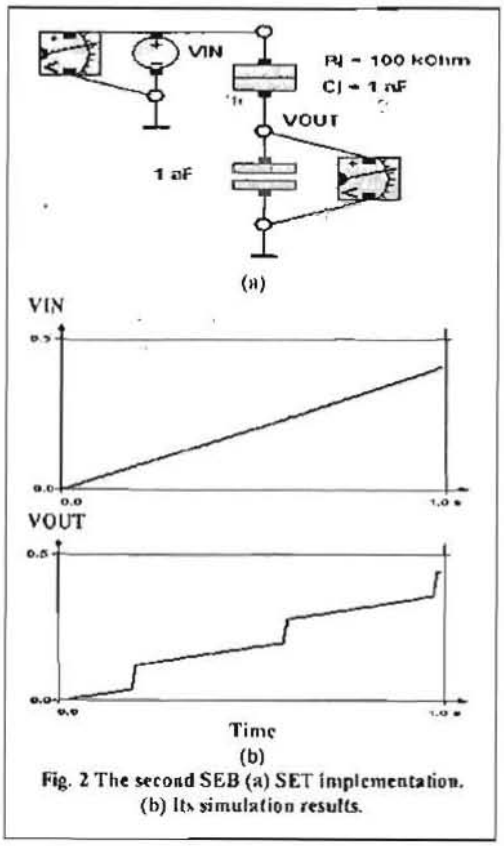


Fig. 2 The second SEB (a) SET implementation. (b) Its simulation results.

3.2 The Linear Threshold Gate:

The general Linear Threshold Gate (LTG) shown in Fig. 3 is able to compute any linearly separable Boolean function represented by:

$$Y = \mathrm{sgn}\{F(X)\} = \begin{cases} 0 \text{ if } F(X) < 0 \\ 1 \text{ if } F(X) \geq 0 \end{cases} \quad (3)$$

$$F(X) = \sum_{i=1}^{n} \omega_i x_i - \psi \quad (4)$$

where x_i are the n Boolean inputs and ω_i are the corresponding n integer weights. The LTG compares between the weighted sum of inputs and the threshold value ψ to determine if the output is logic 1 or logic 0 [7].

Note that this LTG SEC is capable of implementing both positive and negative weights. This can be accomplished by connecting the corresponding inputs (through appropriate capacitors) to nodes POS and NEG (see Fig. 3), respectively.

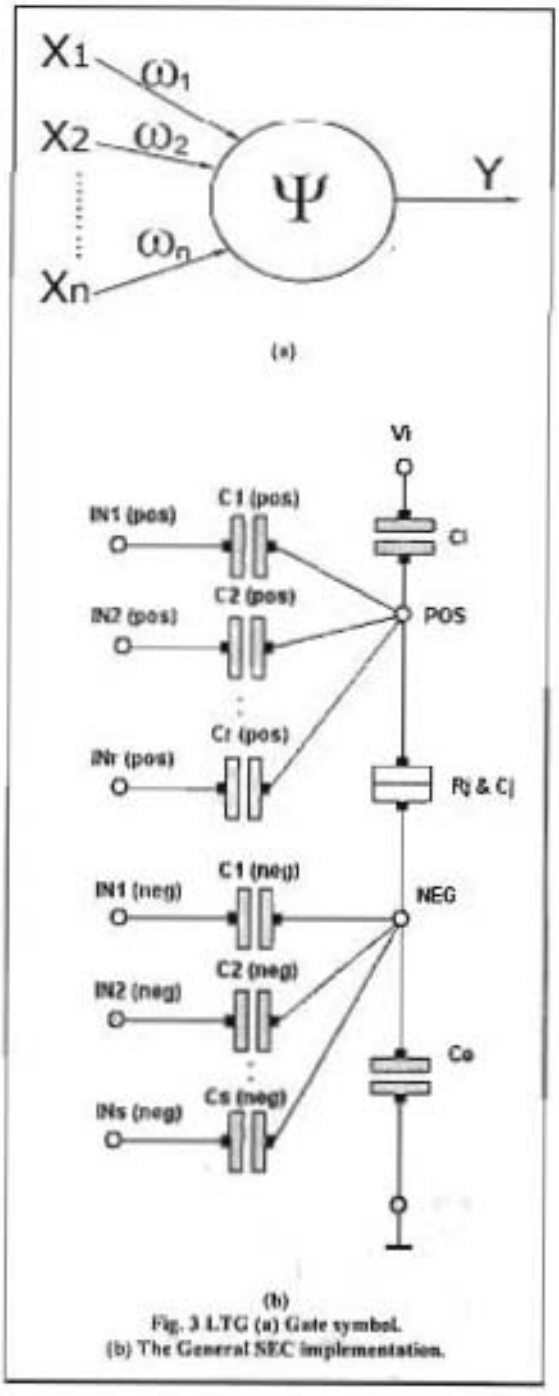
Note also that the threshold value ψ is implemented and can be adjusted by the capacitor C_i and the external voltage V_i.

Due to the passive nature of the LTG circuit, an added buffer/inverter circuit at its output is essential for the correct operation of the LTG circuit. To get both the normal and inverted output, one can add two cascaded inverters at the LTG output [7].

3.3 Boolean Logic Gates:

The basic Boolean logic functions **AND, OR, NAND,** and **NOR** can be implemented as instances of the LTG circuit (described in the previous section) followed by an inverter circuit.

The full design of both the **AND** SEC gate and the **OR** SEC gate are shown in Fig. 4 while the full design of both the **NAND** SEC gate and the **NOR** SEC gate are shown in Fig. 5. The simulation results of the above mentioned four gates using SIMON 2.0 are reported in Fig. 6.



(b)

Fig. 3 LTG (a) Gate symbol.
(b) The General SEC implementation.

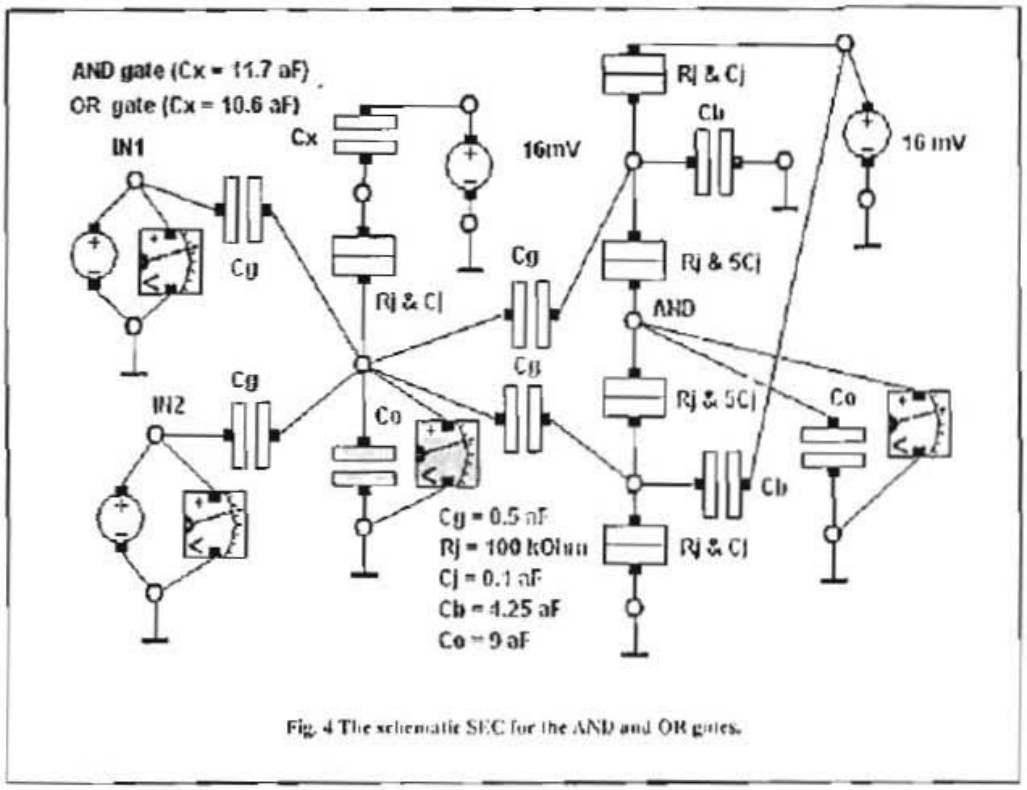


Fig. 4 The schematic SEC for the AND and OR gates.

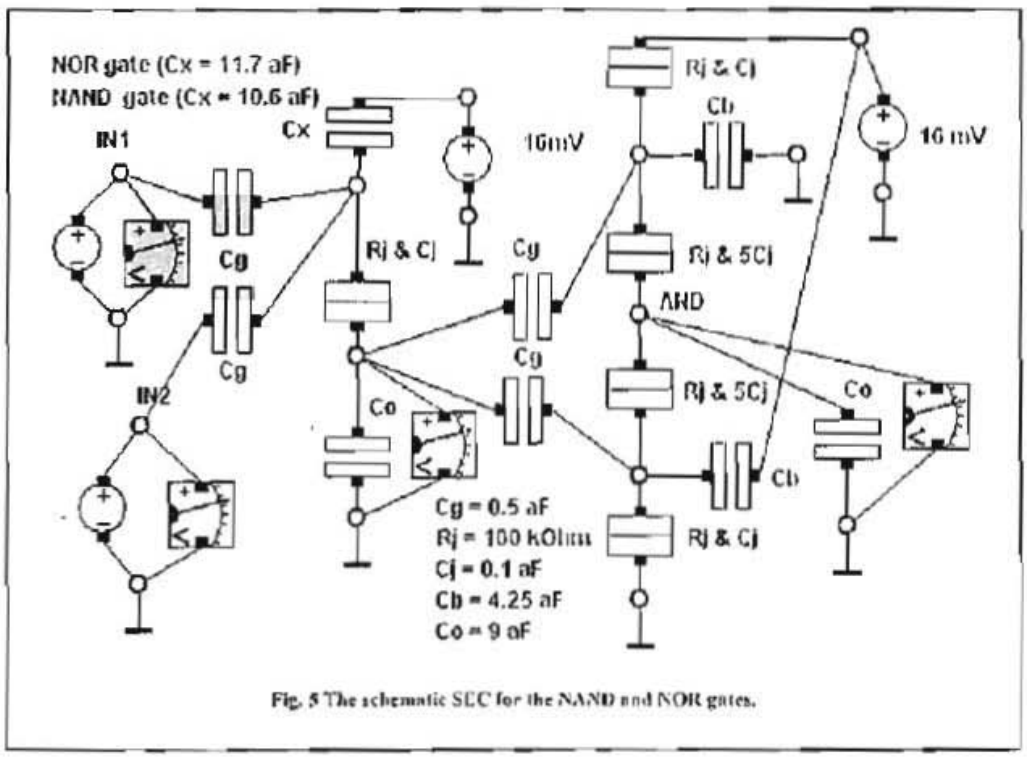


Fig. 5 The schematic SEC for the NAND and NOR gates.

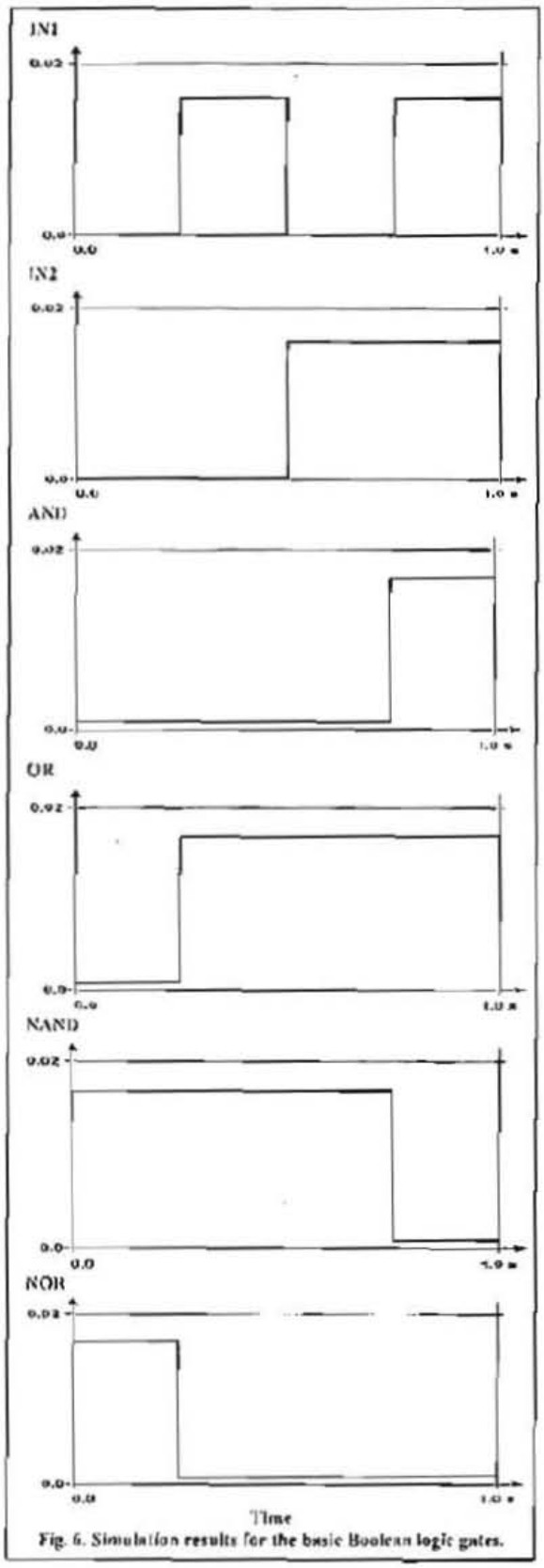


Fig. 6. Simulation results for the basic Boolean logic gates.

4. The Novel XOR SEC:

A two-layer feedforward artificial neural network (ANN) that implements the XOR gate is shown in Fig. 7. The numbers within the neurons represent each neuron's explicit threshold (which can be designed so that all neurons have the same threshold, usually 1). The numbers that annotate arrows represent the weight of the inputs. This net assumes that if the threshold is not reached, zero is the expected output. Note that the bottom layer of inputs is not considered a real neural network layer.

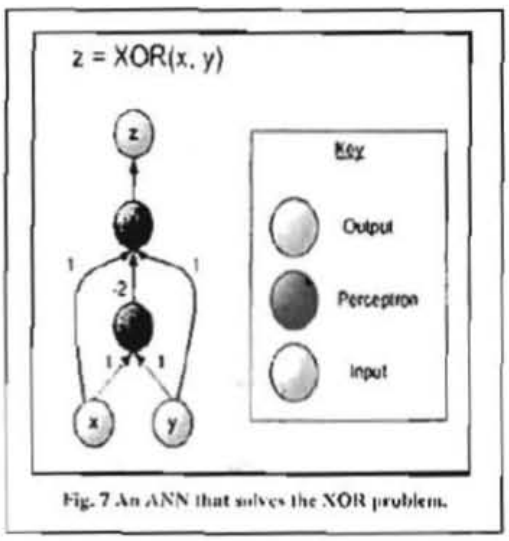


Fig. 7 An ANN that solves the XOR problem.

To implement the above XOR ANN using SET technology, we propose the following:

1. The hidden neuron can be implemented using the AND gate described in sub-section 3.3.
2. The output neuron can be implemented using the general LTG described in sub-section 3.2.

Fig. 8 shows the complete schematic diagram of the developed XOR SET implementation (inc. all parameters used in SIMON 2 simulation).

Note that the output of the AND gate (representing the output of the hidden neuron) is connected to the negative node of the LTG through a ($2C_g$) capacitor (representing the weight –2). Note also that the two other inputs to the output neuron (represented by the two inputs to the SEC) is connected to the positive node of the LTG through a (C_g) capacitor (representing the weight 1).

Fig. 9 shows the SIMON 2 simulation results for the developed XOR SEC. It is worth noting here that this XOR can be used as a half-adder SEC. The XOR output node implements the SUM and the AND node implements the CARRY.

5. Conclusions:

In this paper, some of the basic SEC, found in the literature, was reviewed. SEC (inc. detailed parameters for all used devices) along with the corresponding simulation results (using SIMON 2.0) of these SEC were included. Finally, a novel XOR SEC, with detailed schematic and simulation results, was presented.

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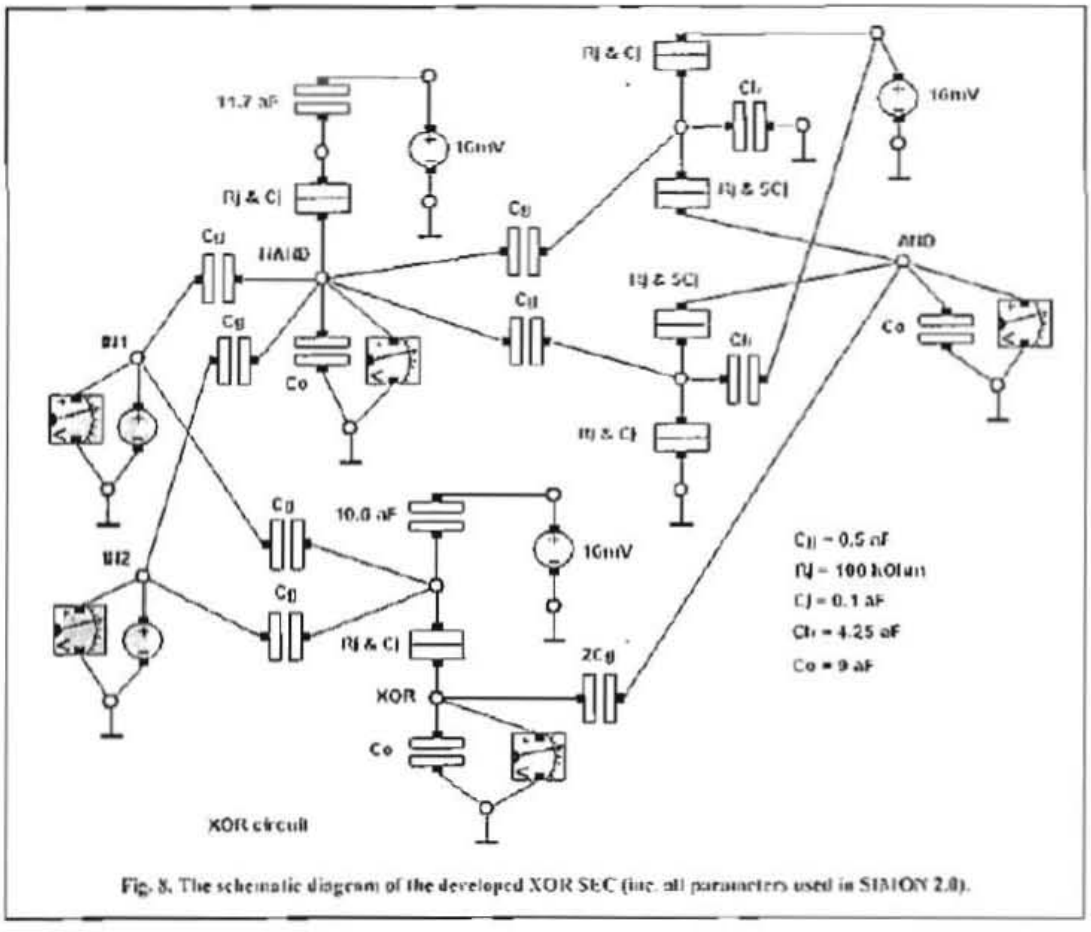

Fig. 8. The schematic diagram of the developed XOR SEC (inc. all parameters used in SIMON 2.0).

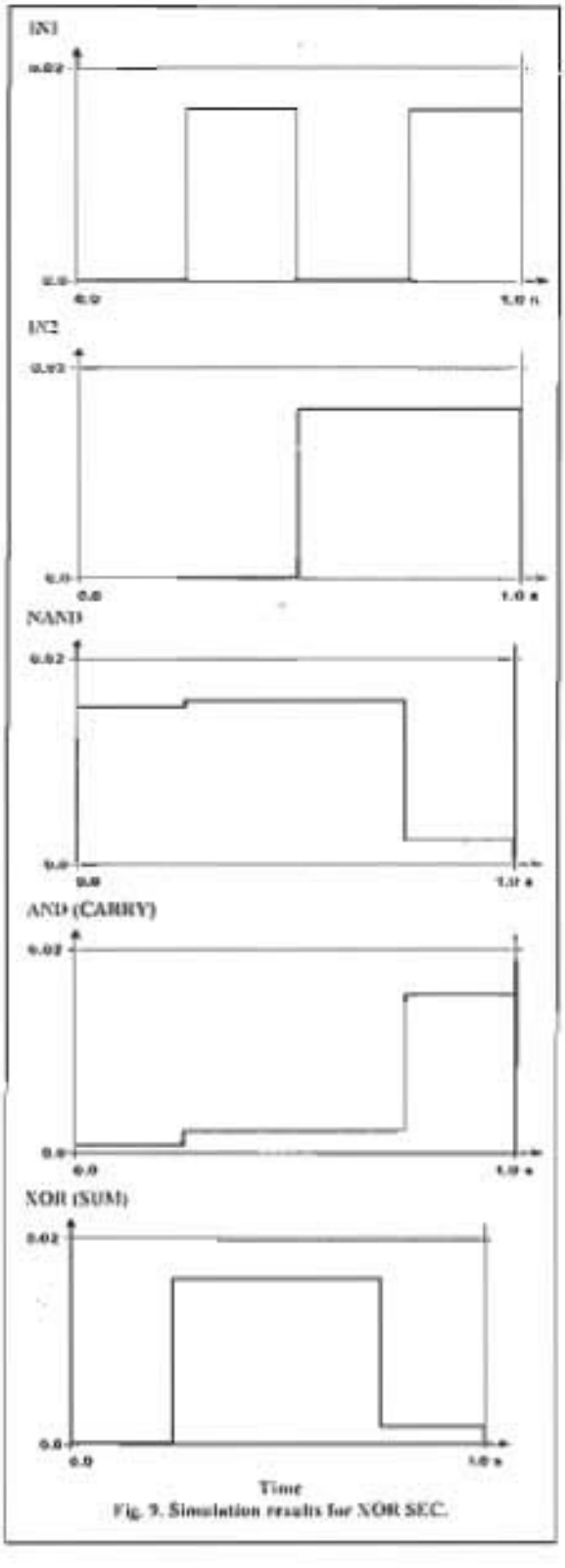

Fig. 9. Simulation results for XOR SEC.

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