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Harmonic Elimination using Discrete Wavelet Transform.

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التخلص من التوافقيات باستخدام DWT

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ملخص: يقدم هذا البحث دراسة عن كيفية عزل محتوى التوافقيات المتواجدة على موجات الجهد والتيار والتى تم تسجيلها فعليا فى المغذيات الخارجة من محطة محولات غرب طلخاالشبكة الموحدة المصرية (٦٦/١١ ك ف). وفى هذا الخصوص تم استخدام طريقة DWT لعمل تحليل لمحتوى موجات الجهد والتيار من التوافقيات. وفى البداية تم عمل محاكاة لمحطة المحولات باستخدام صندوق المعدات فى برنامج "ماتلاب" وذلك فى حالة تواجد مجموعة المكثفات أو عدم تواجدها. وفى هذا المجال تم عمل مقارنة بين موجات الجهد والتيار الناتجة من هذه المحاكاة وبين نظيرتها الفعلية المسجلة فى الموقع. كما تم استخدام النموذج المقترح لدراسة تأثير استبدال مجموعة المكثفات بدائرة توالف لمرشح توازى غير فعال . كما تم تحليل محتوى موجات الجهد والتيار الناتجة باستخدام طريقة DWT المقترحة. و قد أوضحت النتائج تحسن كل من THD لكل من موجات الجهد والتيار وكذلك معامل القدرة .

Abstract: The objective of this paper is to present an approach for isolating the harmonic contents in both voltage and current waveforms at the outage feeder of Gharb Talkha substation (66/11 kV). A novel technique using Discrete Wavelet transform (DWT) for the analysis of the waveforms harmonics content. At the beginning the substation is simulated using Simulink toolbox in Matlab program with and without the presence of capacitor bank. The obtained voltage and current waveforms are compared to the actual data. The proposed model is used to study the effect of replacing the capacitor bank with single tuned parallel passive filter. The resulting current and voltage waveforms are analyzed using the proposed DWT technique. The analysis showed that the Total Harmonic Distortion (THD) of both voltage and current waveforms is improved as well as the power factor.

Keywords: Discrete Wavelet transform (DWT), Harmonic Elimination, Total Harmonic Distortion (THD), and distribution power system.

INTRODUCTION

One of the most important issues for the power system is the reduction of current and voltage harmonics created by non linear loads. Oversizing and derating of the installation is one of the solutions to decrease the effect of harmonics only[1]. Specially connected transformers (star/delta connection) and Zig-Zag transformer are used to isolate triplen harmonics [2].Passive filters series, shunt and series shunt are usually used to filter harmonic current and for reactive power compensation[3,4,5]. The common types of passive filters include single tuned and double tuned resonant filters, but because single tuned resonant filter comprises IC components, it has low investment cost and power loss so it is widely used [6].

Previously, harmonic analysis was done using Fourier transform but recently, Discrete Wavelet Transform (DWT)is utilized. DWT is a mathematical tool to decompose a given signal into different scales at different levels of resolutions [7-9].

In this paper the actual voltage and current waveforms of Gharb Talkha Substation transformer are analyzed using (DWT). This analysis is done with and without the presence of capacitor bank. The substation is then simulated using Simulink Toolbox of Matlab and comparison between actual and simulated voltage and current waveforms is illustrated for both with and without capacitor bank. The proposed model is

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used to detect the effect of replacement of capacitor bank by single tuned parallel passive filter on both the harmonic contents and the power factor.
The following sections presents the problem then the (DWT) technique used for the waveforms after that the simulation and analysis of the results will follow.

Problem Formulation:

The system under study is selected from one of the Egyptian network system. One of the transformers of Gharb Talkha substation (66/11 kV) as a model for studying the harmonics traveling through the system. The transformer is 25 kVA, 66/11 kV, 10 % impedance. In order to improve the power factor from 0.826 to 0.996 at the outer feeder of the substation a capacitor bank of 5.4 Mvar is placed at the low voltage side. The presence of this capacitor bank will cause increase in the Total Harmonic Distortion (THD) of both voltage and current waveforms. The THD of the current waveform is (1.55-5.36 %) without capacitor bank and (3.89-17.48 %) with the presence of capacitor bank while the THD of voltage waveform is (0.85-1.80 %) without capacitor bank and (2.21-4.2 %) with capacitor bank, while the p.f. is improved from (0.826-0.897 lag) to (0.985-0.993 lag).

In order to eliminate such harmonics a single tuned parallel passive filter is connected.

For the design of the filter it is known that the filter impedance is

$$Z_{Fi} = j(X_{Li} - X_{Ci}) \qquad (1)$$

At tuning frequency

$$\frac{X_{Ci}}{n_i} = n_i X_{Li} \qquad (2)$$

Where n is the filter resonant point

$$\therefore X_c = n_i^2 X_L \qquad (3)$$

$$X_{Li} = \frac{1}{n_i^2} X_{ci} \qquad (4)$$

$$Z_{Fi} = \frac{X_{Ci}}{a_i} \qquad (5)$$

Where $$a_i = \frac{n_i^2}{n_i^2 - 1} \qquad (6)$$

Knowing that

$$Z_{Fi} = \frac{1}{S_{Fi}} \qquad (7)$$

$$S_{Fi} = \frac{Q_{Fi}}{S_b} \qquad (8)$$

$$\therefore X_{Ci} = \frac{S_B * a_i}{Q_{F13}} \qquad (9)$$

Where;

Q_{Fi} = the filter reactive capacity
S_b = the base capacity

So the capacitance (C) and inductance (L) for the filter can be expressed as a function of the reactive power compensation (Q_{Fi}) for the filter and the resonant point n_i of each filter.

$$C_i = \frac{Q_{Fi}}{S_B * \omega * a_i} \qquad (10)$$

$$L_i = \frac{S_B * a_i}{Q_{Fi} * \omega * n_i^2} \qquad (11)$$

Discrete Wavelet Transform:

The instantaneous current signal, can be represented by the wavelet transform as follows:

$$i(t) = \sum_k c_{j_0,k}\phi_{j_0,k}(t) + \sum_{j=j_0}^{\infty}\sum_k d_{j,k}\psi_{j,k}(t) \qquad (12)$$

Where;

$c_{j_o,k} = \langle i(t), \phi_{j_o,k} \rangle$ and $d_{j_o,k} = \langle i(t), \psi_{j_o,k} \rangle$

j_o: Scaling level for the lowest band
j: wavelet frequency scales for higher frequency
k: wavelet time scale
c and d: wavelet coefficients
the RMS value for the current I could be obtained as follows:

$$I = \sqrt{\frac{1}{T}\int_0^T i^2(t)dt} = \sqrt{\frac{1}{T}\sum_k c_{j_o,k}^2 + \frac{1}{T}\sum_{j\geq j_o}\sum_k d_{j,k}^2}$$

$$I = \sqrt{I_{j_o}^2 + \sum_{j\geq j_o} I_j^2} \qquad (13)$$

Where I_{jo} is the rms value of the current of the lowest frequency j_o also called *fundamental current* (I_{fun}). $\{I_j\}$ is the set of rms value of the current of each frequency or wavelet-level higher than or equal to the scale level j_o, and are called *harmonic current* (I_h). By the same way the voltage waveform could be analyzed so both voltage and current are

$$V_h = \sqrt{\sum_j V_j^2} \text{ and } I_h = \sqrt{\sum_j I_j^2} \qquad (14)$$

The equivalent total harmonic distortion of voltage THD_V and the equivalent total harmonic distortion of current THD_I can be computed from :

$$THD_V = \frac{V_h}{V_{fun}} \qquad (15)$$

$$THD_I = \frac{I_h}{I_{fun}} \qquad (16)$$

The DWT can used to isolate the frequency band for every signal $S(t)$ having the fundamental frequency f depending on two factors. The first factor is the sample per second of the original signal f_s, while the second factor is the approximation level a_0 and wavelet level d_i where the j is the wavelet level. If the original signal $S(t)$ have the fundamental frequency f = 1 *Hz*, the decomposition level j = 6 level, and the sample per second f_s = 128 *s/s*. Each frequency band could be obtained dividing the sampling frequency by two (128/2=64). Table (2) shows the approximation, details, and frequency band for the signal $S(t)$. A_5 is the approximation containing the DC component, fundamental, and second harmonic. The level D_5 to D_1 is the detailed components for the signal at each frequency as in table (1).

Table (1) Wavelet level and frequency bands for sampling (128 *S/S*)

$F_s = (2^7 * 1) = 128$ sample / second			
Levels		Frequency bands	Odd harmonics
j_o	A_5	(0-2)	DC + Fundamental + second harmonic
j	D_5	(2-4)	(2^{nd} to 4^{th})harmonic
	D_4	(4-8)	(4^{th} o 8^{th}) harmonics
	D_3	(8-16)	(8^{th} to 16^{th})harmonics
	D_2	(16-32)	(16^{th} to 32^{nd}) harmonics
	D_1	(32-64)	(32^{nd} to 64^{th}) harmonics

When using different sampling frequencies 2^8*f, 3*2^7*f, 2^9*f where f is the fundamental frequency, the different harmonics could be calculated as follows:

$$S_1 = A_{5(128)} \qquad (17)$$

$$S_3 = \sqrt{A_{5(256)}^2 - A_{5(128)}^2} \qquad (18)$$

$$S_5 = \sqrt{A_{5(384)}^2 - A_{5(256)}^2} \qquad (19)$$

$$S_7 = \sqrt{A_{5(512)}^2 - A_{5(384)}^2} \qquad (20)$$

$$S_9 = \sqrt{A_{5(640)}^2 - A_{5(512)}^2} \quad (21)$$

$$S_{11} = \sqrt{A_{5(768)}^2 - A_{5(640)}^2} \quad (22)$$

$$S_{13} = \sqrt{A_{5(896)}^2 - A_{5(768)}^2} \quad (23)$$

Where $A_{m(n)}$ is the m approximation when the sampling frequency is n times the fundamental frequency.

Simulation and Analysis of Results:

In order to study the effect of filter placement on both voltage and current waveforms, simulation of Gharb Talkha substation is carried on using Simulink toolbox of Matlab. The output of the simulation could be seen in comparison with the actual data in Figures 3,4.

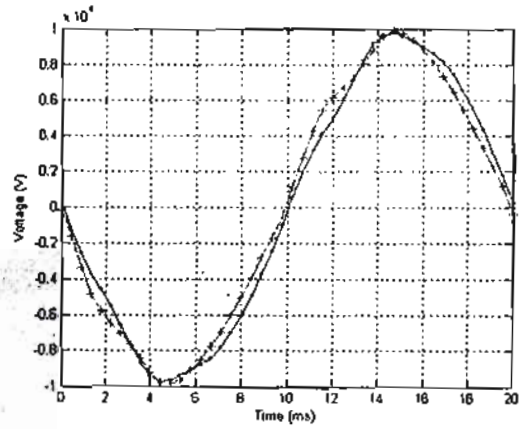

Figure (3) Actual(+) and Simulated (-) voltage waveform

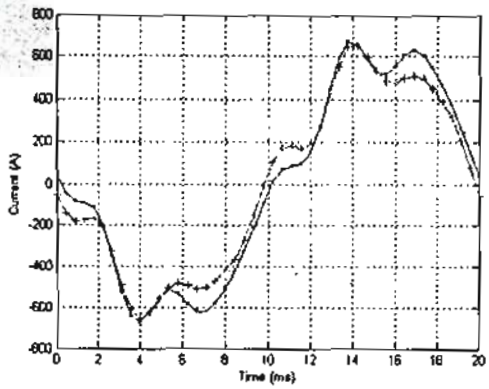

Figure (4) Actual(+) and Simulated (-) current waveform

It could be seen that there is almost no difference between actual and simulated output waveforms.

The single tuned parallel passive filter is designed according to equations (1-16) and the data is seen in Table (2)

Table (2) Filter parameters.

	Filter (5)	Filter (7)
Harmonic number (h)	5th	7th
Line voltage V_L (kV)	11.4	11.4
Resonance point n_h	h_5 = 4.6	h_7= 6.44
Q_{1h} (MVar)	Q_{15}=3.27	Q_{17}= 2.13
R_h (Ω)	0.0906	0.097
C_h (μF)	76.3067	50.912
L_h (mH)	6.275	4.7985

When these filters are connected at the bus bar substation as shown in Figure (5), the result of DWT for current using 128*50 sampling rate is shown in Figure (6).

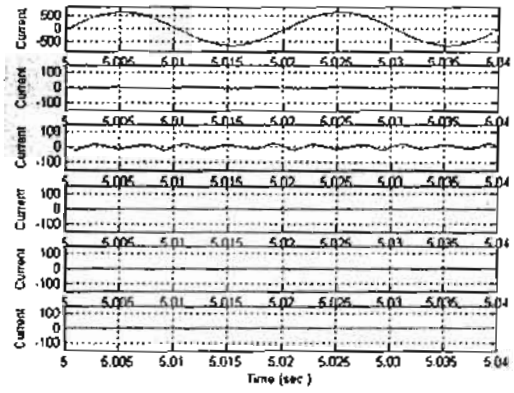

Figure (6) Detailed and pproximation of current waveform with 128*50 sampling frequency.

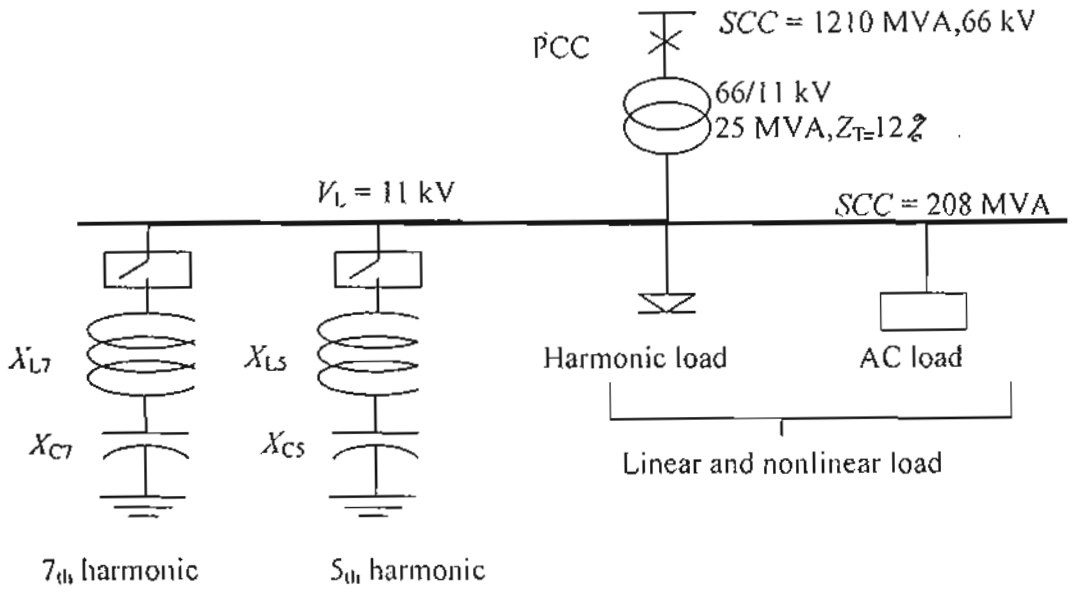

Figure (5) The substation with the filters connected to it.

Using equations (17-23) for the analysis of the waveforms revealed the results shown in Tables (3,4) for both voltage and current.

Table (3) Current signal analysis using DWT

I_1	446.15	A	I_7	3.2	A
I_3	3.63	A	I_{total}	446.3	A
I_5	11.8	A	THD_I	2.9	%

Table (4)Voltage signal analysis using DWT

V_1	6737.75	V	V_7	12.25	V
V_3	6.2	V	V_{total}	6738	V
V_5	34.18	V	THD_v	0.56	%

It could be seen from the above results that the THD for the current decreased from (3.89-17.48 %) with the presence of capacitor to about 2.9 % and for the voltage the THD decreased from (2.21-4.2%) with the capacitor to about 0.56 % with the filter presence. Also it should be noted that the p.f. reached a value of with the presence of the filter 0.994.

Conclusion:

A novel technique for isolation of different types of harmonics using DWT with different sampling rate is implemented. Parallel passive single tuned filters of fifth and seventh order are used to eliminate the harmonics and improve the p.f. as well. The suggested DWT is used to analyze the voltage and current waveforms of Gharb Talkha substation. The results showed that the THD for both voltage and current waveforms is decreased and the power factor is improved.

1- Introduction

Automatic digital modulation recognition is a rapidly evolving area in communication system research where it covers many interesting applications in both civilian and military domains. These applications include signal monitoring, interference, intelligent modems, spectrum management, military threat detection and adaptive wireless communications[2]

Modulation recognition is an essential part in software radio[3,4], where the modulation scheme can be varied according to channel capacity, and a receiver with automatic modulation recognition is required to detect the modulation scheme in real time.

Many techniques for AMR have been published which are divided into three categories:

1- Decision theoretic approach
2- Pattern recognition approach
3- Combined approach

In decision theoretic approach the classification depends on signal envelope characteristics, zero-crossing, likelihood functions, and other statistical parameters like moments[5,6].

Pattern recognition approach is based on the principle of pattern recognition techniques which include signal preprocessing, features extraction, and finally the classifier. Many researches used artificial neural network (ANN) as the classifier in modulation recognition for different types of digital modulation schemes[7,8,9,10].

A combined approach which uses more than one technique for modulation classification such as Fuzzy logic with statistical moment[11], hierarchical classification using cumulants[12], Discrete Fourier Transform (DFT) with phase histogram[13], joint phase lock detection and identification[14], fuzzy logic with genetic algorithm[15], and neural networks with higher order statistics[16].

Also there are some approaches which depend on the implementation method. For practical reasons considering complexity and hardware size, most of the previous algorithm can not be implemented for real time processing, so another simplified approaches are adopted to make the implementation feasible using hardware platforms like FPGA, Digital Signal Processors, and Microcontrollers.

This work is focused on the use of FPGA as the hardware platform for the implementation of AMR algorithm which can classify the major types of digital modulation (ASK, FSK, and PSK).

The choice of FPGA as the platform for the implementation is based on the fact that it has many advantages over other platforms. FPGA can be

used as a reconfigurable hardware to be adapted for various modulation schemes with the aid of simple microcontroller circuit and memory to hold the configuration data.

FPGA is based on hardwired logic circuits which provide a very high processing speed which is needed for communication signal processing. It also has the advantage of being software programmable using HDL (High Descriptive language) over discrete hardwired circuits which need complex design techniques.

2-Proposed Technique

The aim of the work is to present an algorithm of AMR for digital modulation schemes that can discriminate between 16-level QAM, 16-ary FSK, and 16-ary PSK.

Each type of the three signals is assumed to have the same carrier frequency. Other parameters like sampling frequency, carrier frequency, and synchronous carrier needed for signal processing are generated using analog front end processor.

All treated data are the samples of the incoming signal taken at a rate determined by the front end processor. These samples are constrained to 8-bit word length including the sign bit.

The block diagram of the proposed system is shown in Fig. 1. The signal is analyzed to its main parameters amplitude, phase, and frequency. These parameters are then analyzed using decision block to measure the variations in each parameter separately, then the system decides which type of modulation is present.

Only one of the three possible outputs will be active FSK, ASK or PSK, also the degree of modulation will be available as a binary code through data outputs $D_3D_2D_1D_0$ which represent a number from 1 to 16; for example if the modulation detected is PSK, and DATA= (0010), this means that it is a 2-ary PSK.

The following discussion explains the construction of each block in more details.

2.1 ASK Modulation

ASK modulation detection is based on observing the amplitude of the incoming signal and analyzing it to determine if there is any amplitude variation. If amplitude variation is observed then the next step is to decide the number of possible amplitudes the signal can have (degree of modulation).

Fig. 2 shows the block diagram of the proposed amplitude detection circuit. The signal is first squared and then averaged over one period to give an indication of signal amplitude as follows:

$$y_1 = A^2\left(\cos(\omega_c t + \theta)\right)^2$$
$$= \frac{A^2}{2}\left(1 + \cos(2\omega_c t + 2\theta)\right) \quad (1)$$

$$y_2 = \frac{A^2}{2} \quad (2)$$

We get y_2 which is proportional to amplitude of the incoming signal, and the next step is to determine if this amplitude is almost constant (no modulation present) or varies between different values.

Another block is as added to perform amplitude analysis is shown in Fig. 3. The 16-value discriminator is used to analyze the amplitude variation to determine the presence of modulation and its degree. The amplitude values are averaged and stored in 8-bit register. Only the 4 high order bits is used to measure amplitude variation, and this gives a 16 possible amplitude values.

The 4 to 16 decoder will activate one of its outputs according to the value of the incoming amplitude. This active signal is used to increment a counter associated with this amplitude to count the number of occurrence of each amplitude value over 96 cycles. Finally after 96 cycles the 16 to 5 encoder gives a number from 1 to 16 indicating the degree of modulation if present. To clarify this function, consider that the modulation has a degree of 4 then signal amplitude will vary between 4 different values (A_1, A2, A3, A4). Now if the current amplitude is A_i (i=1,2,3,4) then counter$_i$ will be incremented and finally after 96 cycles we get only 4 nonempty counters indicating that a modulation is present and its degree is 4. If only we get one non-empty counter, this indicates that there is one signal amplitude (no amplitude variations), and the 16 to 5 encoder will indicate that no modulation is present.

The 3rd bit of each counter is used to indicate if the counter is full or empty. The design of the 16 to 5 encoder is simplified using a 16 bit adder, where the number of full counters is summed to give an indication of the modulation degree.

2.2 FSK Modulation

Fig. 4 shows the details of the frequency detector block, where a counter with fixed clock frequency is used to measure the period of each signal cycle.

A zero cross detector is used to trigger the counting operation by observing the signal variation from negative value to positive value, and this can be simplified by using the sign bit of the input signal (1 negative value- 0 positive value) as the counter enable signal. After each cycle the counter value is latched into a register to be processed further to determine if modulation is present and the degree of modulation, and this can be done using the same block (16-value discriminator) used in ASK detection.

2.3 PSK Modulation

The proposed system for m-ary PSK modulation detection is based on measuring the phase difference θ by using synchronous demodulator as shown in Fig.5 where:

$$y_1 = A^2 \cos(\omega_c t)\cos(\omega_c t + \theta) \quad (3)$$

$$y_1 = \frac{A^2}{2}\left(\cos(2\omega_c t + \theta) + \cos(\theta)\right) \quad (4)$$

Now after the low pass filter (LPF) the first term will be filtered out and we get

$$y_o = \frac{A^2}{2}\cos(\theta) \quad (5)$$

The output now is proportional to the phase difference θ and can be used to measure the angle of the incoming signal, but this angle is restricted to values between 0 to 180 degree where we can't distinguish a phase difference of 90 and -90 degree.

So we must add another parameter to extend the range of measurements to any value between 0 and 360 degree. Another branch is added as shown in Fig. 6

We have two outputs:

$$y_{o1} = \frac{A^2}{2}\cos(\theta) \quad (6)$$

$$y_{o2} = \frac{A^2}{2}\sin(\theta) \quad (7)$$

The first output can be used to measure the value of the phase difference and the other output is used to determine the polarity of the phase difference and hence we can measure a phase difference between -180 and up to 180 degree.

The implementation of the proposed m-ary PSK modulation detection using FPGA module must be modified to satisfy the design consideration and capabilities of FPGA.

The main functions of the proposed technique are:

1- Multiplication
2- Low pass filtering

2.3.1 Multiplication

The proposed technique needs to multiply two sampled signals quantized by 8 bits each. This multiplication will consume most of the FPGA cells if it is implemented by direct hardware multiplier, where a multiplication of two operands of 8 bits each require an array of 8×8 full adders which will consume large amount of FPGA cells.

So another technique is used to perform multiplication using memory lookup tables, where the values of multiplication can be stored in a memory for each expected combination of input values. For 8×8 multiplication we will need 2^{16} memory location.

The multiplication process in the proposed algorithm must be modified to make the implementation using FPGA module more convenient. Fig. 7 shows how to perform signal multiplication using indirect method that will lead to more efficient use of FPGA.

$$y_1 = A\left(\cos(\omega_c t) + \cos(\omega_c t + \theta)\right) \quad (8)$$

$$\begin{aligned} y_1^2 &= A^2\left(\cos(\omega_c t) + \cos(\omega_c t + \theta)\right)^2 \\ &= A^2\begin{pmatrix} \left(\cos(\omega_c t)\right)^2 + \left(\cos(\omega_c t + \theta)\right)^2 \\ +2\left(\cos(\omega_c t)\right)\left(\cos(\omega_c t + \theta)\right) \end{pmatrix} \\ &= A^2\begin{pmatrix} \frac{1}{2}\left(1 + \cos(2\omega_c t)\right) + \\ \frac{1}{2}\left(1 + \cos(2\omega_c t + 2\theta)\right) + \\ \left(\cos(\theta)\right) + \left(\cos(2\omega_c t + \theta)\right) \end{pmatrix} \end{aligned} \quad (9)$$

After the LPF we get,

$$y_{o1} = A^2\left(1 + \cos(\theta)\right) \quad (10)$$

Similarly the orthogonal branch shown in Fig. 8 will produce,

$$y_{o2} = A^2\left(1 + \sin(\theta)\right) \quad (11)$$

The squaring process can be implemented in FPGA using lookup table with 8-bits input and a normalized 8 bits output will require 256 bytes of memory space.

The same table can be duplicated to calculate the output of the second branch.

2.3.2 Low pass filtering

The design of LPF using DSP techniques like finite impulse response filter (FIR) will consume large amount of the FPGA chip, so we simplify the design of the filter by using the average process over one period of the input signal that will be suitable for FPGA implementation.

Fig. 9 shows the block circuit of average filter used to reject the high frequency terms and the noise from the processed signal

3 Results and Discussion

The proposed system was built using Xilinx Spartan-3 platform FPGA development kit which contains 200,000 gates Platform FPGA XC3S200-4FT256C Chip. The development kit contains 1M-byte of fast asynchronous SRAM which is used to store the lookup tables needed for implementation.

Table 1 shows FPGA usage for each type of modulation recognition used in the implementation. The FPGA usage is measured in units of CLB (Configurable Logic Block) which is the smallest functional block.

Also the maximum clock frequency that the implementation can handle is indicated in Table 1. This frequency

indicates how fast the system for real time applications.

The proposed system needs 979 CLBs to be implemented which can be fitted in one large sized FPGA like Spartan-3. The clock frequency is limited to 77.3 MHz to accommodate the PSK detection requirements and is adequate for real time system.

Also since the entire AMR algorithm is fitted in one chip FPGA, there will be no need to reconfigure the chip for each modulation type like other system[17].

The system was tested using a test setup consisting of microcontroller based signal generator and a lookup memory for modulation selection. The test signal is sampled at 20 MHz sampling rate. The digital data is taken from a predefined file stored in the ROM of the microcontroller with data rate of 512 kbps.

The proposed squaring process reduces the signal to noise ratio at the output of the multiplier and this affect the maximum degree of modulation that the system can handle. A modification is added to the system to reduce the noise by increasing the resolution of the multiplier using 12 bit lookup tables and filters. Increasing the resolution to reduce system noise enables the system to handle modulation degree up to 16 levels without errors, but a remarkable increase in CLB usage is observed. Fortunately the total CLB usage is within the limit of the SPARTAN-3 FPGA chip (1020 CLBs).

Further increase in the degree of modulation will need a larger chip or the use of two chips to enable higher resolution.

The proposed system was tested under noisy environment with SNR of 10 dB and the success rate is 100% (without errors). This result represents a performance advantage over previous researches in AMR [9,15,16,17].

4 Conclusion

The proposed system and FPGA implementation of AMR works successfully for ASK, FSK, and PSK. Modulation degree up to 16-ary was achieved without error. Only one FPGA chip is used for implementation without the need for reconfiguration process which increases the detection time. The proposed system proves that FPGA can be a suitable platform for AMR implementation for real time application and with the increasing progress in the development of FPGA architecture more modulation scheme can be fitted in a single chip. Also the implementation of demodulators can be easily achieved with simple modification of the proposed hardware. So a complete module of demodulator with AMR can be implemented using FPGA hardware suitable for many applications such as software radio.

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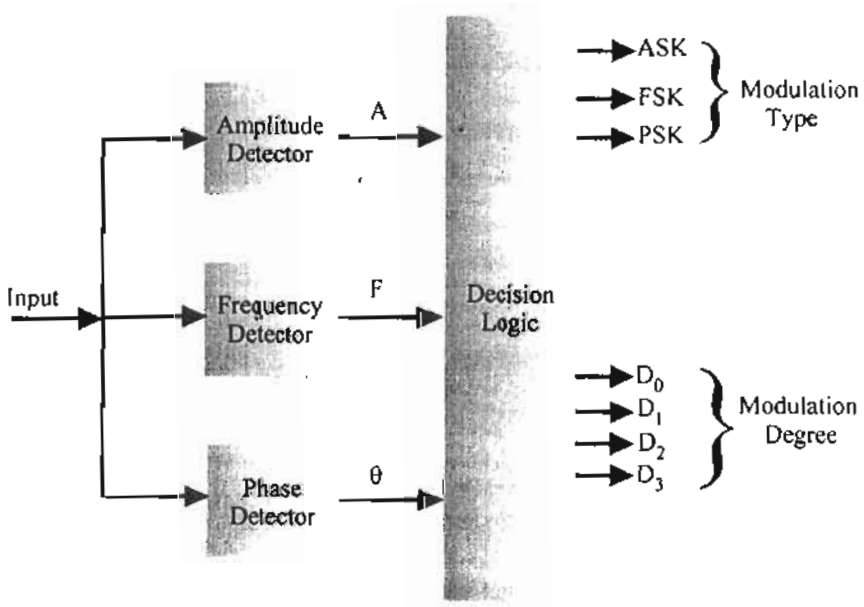

Figure 1 Block Diagram of Modulation Detection

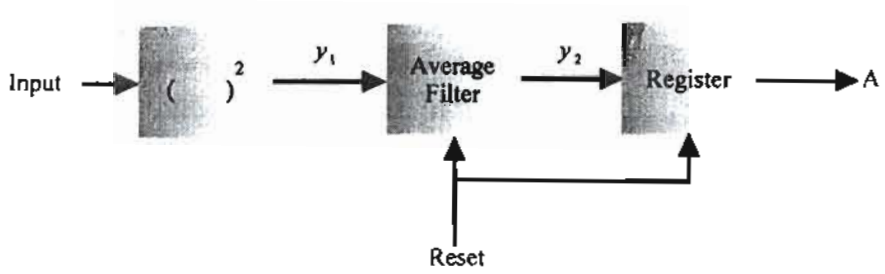

Figure 2 Block Diagram of ASK Detection

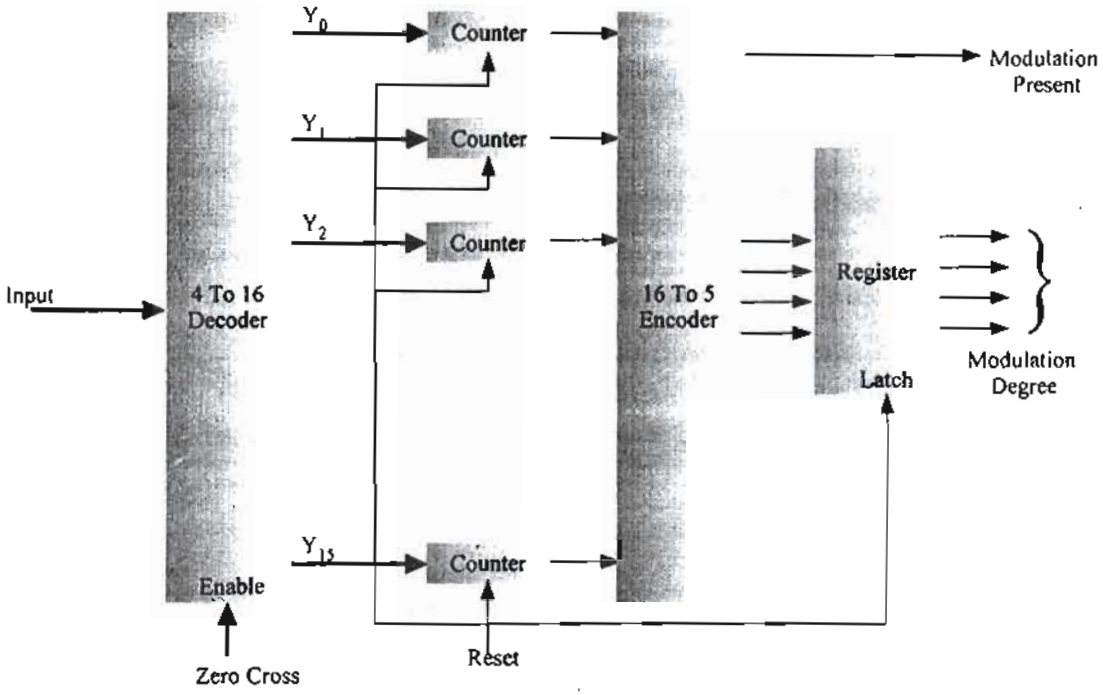

Figure 3. Block Diagram of 16 value discriminator

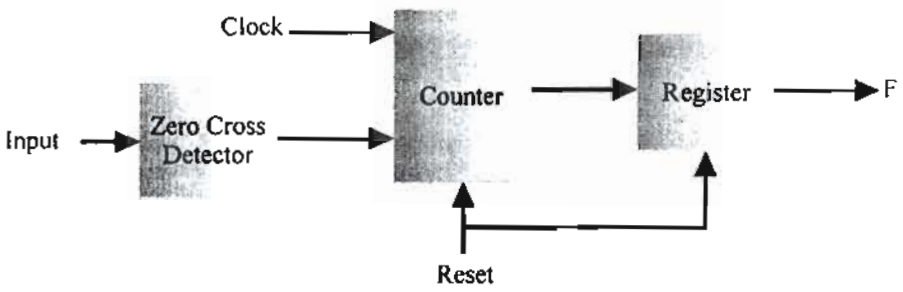

Figure 4. Block Diagram of FSK Detection

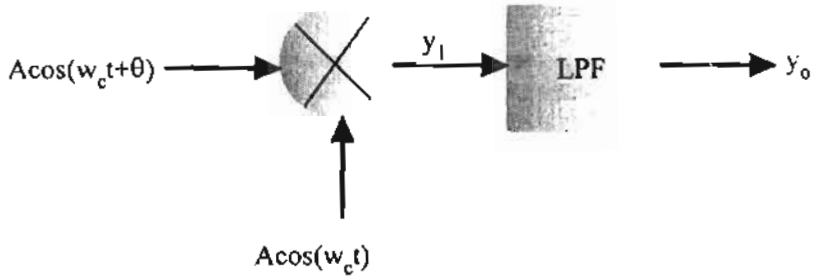

Figure 5. Block Diagram of simplified PSK Detection

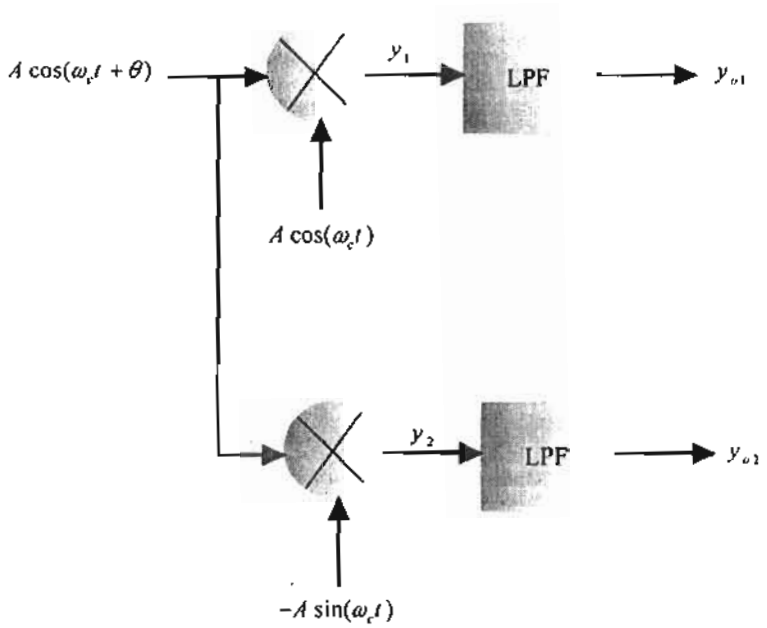

Figure 6. Block Diagram of proposed PSK Detection

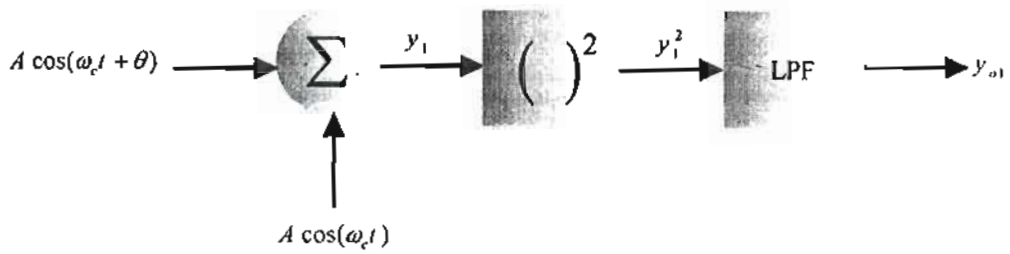

Figure 7 Block Diagram of multiplication process

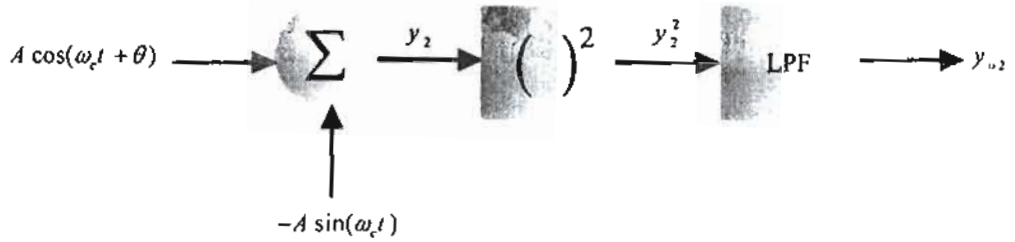

Figure 8 Block Diagram of multiplication process in the orthogonal branch

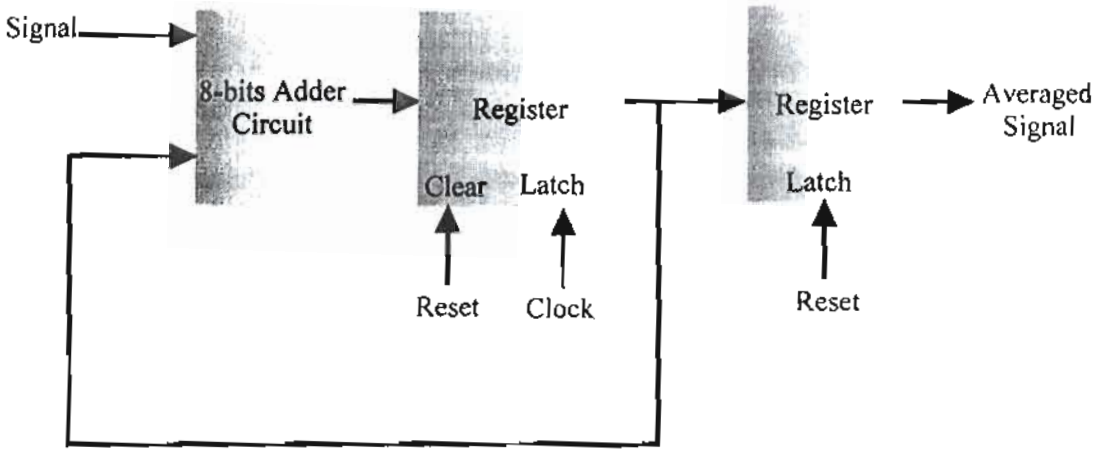

Figure 9 Block Diagram of the average filter

Table 1 Performance measure (CLB usage and Maximum usable frequency)

Performance / Modulation	CLBs / Max CLBs	Max Frequency Mhz
ASK	301/1024	81.7
FSK	215/1024	95
PSK	463/1024	77.3