Mansoura Engineering Journal

Volume 40 | Issue 1 Article 2

7-5-2020

Improved Hybrid SET/MOS Digital-Analog and Analog-Digital Converters.

Lobna Osman
Communications and Electronics Engineering Department, Faculty of Engineering, Mansoura University (MU), Mansoura, EGYPT 35516

Sameh Rehan
Communications and Electronics Engineering Department, Faculty of Engineering, Mansoura University (MU), Mansoura, EGYPT 35516

Abdel-Fattah Abdel-Fattah
Communications and Electronics Engineering Department, Faculty of Engineering, Mansoura University (MU), Mansoura, EGYPT 35516

Improved hybrid SET/MOS Digital-Analog and Analog-Digital Converters

المحولات الرقمية التناظرية و التناظرية الرقمية المحسنة باستخدام الدوائر المختلطة (SET/MOS)

Eng. Lobna A. Osman, Prof. Sameh E. Rehan, and Prof. Abdel-Fattah I. Abdel-Fattah
Communications and Electronics Engineering Department,
Faculty of Engineering, Mansoura University (MU), Mansoura, EGYPT 35516
Corresponding author:
E-mail: englobna20@yahoo.com Tel.: +20 1094704854

ملخص البحث

دوائر تحويل الإشارات الرقمية والتناظرية هي دوائر مهمة، لأنها يمكن أن تستخدم في أنظمة معالجة الإشارات، وأنظمة معالجة الصورة وأنظمة الاتصالات. معظم الباحثين في الوقت الحاضر مهتمين بكيفية الحد من تبديد الطاقة وبناء الدوائر المدمجة، وزيادة سرعة التحويل .هذا البحث يقدم نوعين من المحولات الرقمية التناظرية و التناظرية الرقمية المحسنة باستحدام الدوائر المختلطة SET/MOS.

دوائر المحولات الرقمية التناظرية و التناظرية الرقمية المختلطةSET/MOS لديها مزايا دائرة SET و دائرة MOS. تم استخدام نموذج PSPICE العلاقة التكرارية (RRM) مع أربع حالات للشحنة للترانزستور أحادى الالكترون.

تم محاكاة دوائر المحولات الرقمية التناظرية النانوية المختلطةSET/MOS المحسنة (على ن = 4 و 8) باستخدام جهاز المحاكاة PSPICE ORCAD Capture. تم محاكاة دوائر المحولات التناظرية الرقمية المختلطة SET/MOS (على ن = 3 و 8). اظهرت النتائج ان دوائر المحولات الرقمية التناظرية و التناظرية الرقمية المحسنة المقترحة لها مميزات وهى قدرة القيادة العالية وتحسين اشارة الخرج التى هى احسن من دوائر المحولات التى تستخدم الترانزستور احادى الالكترون فقط. دوائر المحولات الرقمية التناظرية لديها شكل الدوائر المدمجة وارتفاع كثافة التكامل والسرعة العالية وارتفاع قيادة الحمل وفقد اقل للقدرة مقارنة مع دوائر مختلطة تستخدمSET/MOS ذكرت سابقا.

Abstract

Digital and analog signal conversion circuits are important circuits as it can be used in signal processing systems, image processing and communication systems. The most researchers nowadays are interested with how to reduce power dissipation, compact circuit structure, and increase the speed of conversion. This paper present two types of improved hybrid SET/MOS DAC and ADC circuits. The SET/MOS hybrid ADC and DAC circuits have the advantages of the SET circuit and the MOS circuit. The PSPICE Recursion Relation Model (RRM) with four charge states of the SET transistor was used. The improved hybrid n-bit DAC nano-circuits are simulated (for n = 4 and 8) using Orcad Capture PSPICE simulator. The performance of the SET/MOS hybrid n-bit ADC circuits were simulated (for n = 3 and 8). The results show that the proposed improved n-bit DAC and ADC nano-circuits have the advantages of high driving capability and the enhanced swing of the output signal which is better than pure SET ADC and DAC circuits. The improved n-bit DAC nano-circuits have compact circuit structure, higher integration density, high speed, high load drivability, and low-power dissipation compared with the previously reported SET/MOS hybrid DAC.

Keyword

Single Electron Transistor (SET), MOS transistor, Nano-circuits, hybrid, Analog-Digital Converter (ADC) , Digital-Analog Converter (DAC), Recursion Relation Model (RRM), room-temperature, PSPICE.

Received: 24 June, 2014 – Revised: 29 October, 2014 - Accepted: 31 December, 2014

1. Introduction

Feature size reduction in microelectronic circuits has been an important factor to the dramatic increase in the processing power of computer arithmetic circuits. However, it is generally accepted that sooner or later MOS based circuits cannot be reduced further in feature size due to fundamental physical restrictions [1]. The rapid progress in the fabrication technology of silicon nano devices has pushed the device dimension toward nanometer scale. When device dimensions are reduced to a few nanometer range, the single electron tunneling leads to interesting new device characteristics. If we wished to continue obeying the Moore law and make the circuits cheaper, faster and the power dissipation lower, some new electronic devices would have to be created, such as Single-Electron Transistor (SET)[2]. Single Electron Transistor (SET) is expected to be the future of VLSI design due to its nanoscale feature-size, ultra low power dissipation and high density. Compared with other nano-devices, SET is a new device because of its advantages of little size, low operating power, high integration and easy to combine with MOS[3]. The fundamental principle of single-electronic is the Coulomb blockade, which was first observed and studied by Gorter [4]. Pure SET circuits have very limited applications due to SET's low current drivability, small voltage gain and low-temperature operation, since MOS devices have advantages that can compensate for the disadvantages of SET, hybrid SET/MOS architecture which combines the advantages of both MOS and SET. Tunnel junction is the basic unit cell in Single Electron Transistor. It consists of two pieces of metal separated by a very thin (~1nm) insulator [2]. The basic single-electron nano-devices is the tunnel junction which can be thought of as a leaky capacitor, through which the movement of individual electrons can be controlled [23]. Fig. 1 shows the symbol of a SET device. It consists of two tunnel junctions in series sharing a common electrode, which is called the island, also known as the quantum dot and two gates are coupled to the island. Any single-electron (SE) circuit has at least one floating node, between connected tunnel junctions and/or capacitors, that is called an island or a quantum dot (QD) [24].

The orthodox theory is the description of charge transport utilizing free energy, tunnel rates, coulomb blockade and quantization of charge transport [25].

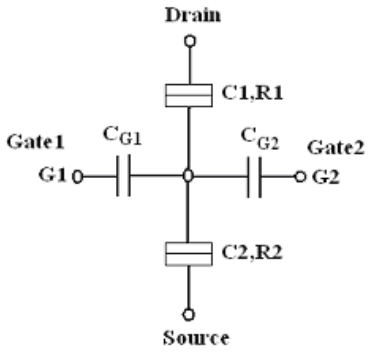

Fig. 1. Single Electron Transistor symbol

Lientschnig et al. 2003 [5] introduced an exact model for Single-Electron Transistor and named it Recursion Relation Model (RRM). This model uses the orthodox theory of single-electron tunneling and determines the occupation probabilities of states. The RRM model is shown in Fig. 2, which consists of two tunnel junctions, two gates are coupled to the island, a voltage source is connected to the source, the drain, and the two gates. This model uses eleven charge states. In this paper, RRM model with four-charge states were used in the simulation to reduce the time, current and the power dissipation using OrCAD Capture PSPICE. The current-voltage characteristics (I_D-V_{DS}) of the SET at V_{GS}=0.02V are shown in Fig. 3 using four-states RRM model by OrCAD Capture PSPICE.

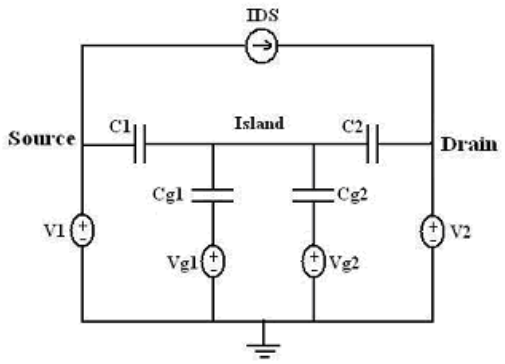

Fig. 2. Single Electron Transistor model in PSPICE

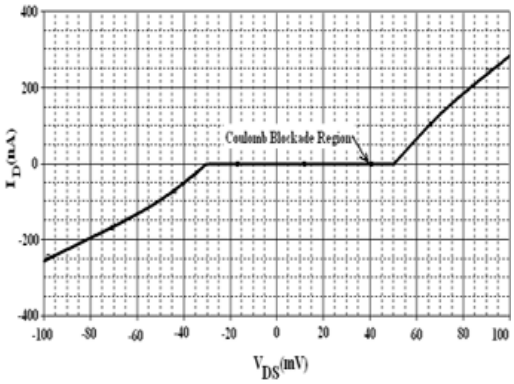

Fig. 3. The current-voltage characteristics (I_D-V_{DS}) of the SET

Digital and analog signal conversion circuits are useful circuits, it can be used in signal processing systems, image processing and communication systems. The Analog-to-Digital Conversion (ADC) and Digital-to-Analog conversion (DAC) are developed to obtain high integration density, high speed, and low power dissipation. The advantages of ADC and DAC circuits which uses Single Electron Transistor are low power dissipation, high integration density and high speed. Some research groups had proposed several kinds of ADC and DAC circuits based on SET [6]–[11]. An improved hybrid SET/MOS DAC and ADC circuits were presented in this paper to take the advantages of the proposed SET/MOS architecture for high temperature operation and driving capability. Their advantages are low power dissipation, small size, circuits have large load capability and large signal swing. In this paper, DAC using hybrid SET/MOS circuit is illustrated in section 2. ADC using hybrid SET/MOS circuit is introduced in section 3. ADC circuit using SET is simulated in section 4. Finally, conclusions are given in section 5 followed by the references.

2. DAC using hybrid SET/MOS circuit

2.1. Operating principle for n-bit hybrid SET/MOS DAC circuit

Fig. 4 shows the basic schematic of an n-bit hybrid SET/MOS DAC circuit. It consist of two parts, the first part is a signal input capacitive array block, the second part is a Single Electron Transistor in series with depletion type NMOS (output block). The ratio of capacitor's values is 2^0:2^1:2^2:2^3:….: 2^n in the capacitance array.

When an n-bit digital signal D_0,D_1,D_2,…….D_{n-1} is applied to the capacitance array (first part), the output of the capacitance array is connected with the input of the output circuit (second part) which consists of SET in series with NMOS. The NMOS transistor M_1 acts as the load of SET, its gate is connected with the source. In this circuit Single Electron Transistor was used with two gates, the first gate (G_1) acts as signal input end; the second gate (G_2) is used to control the phase of SET. The second gate of SET (G_2) also has the function to compensate the background charge. This circuit structure was proposed by authors in [12], [13].

The input gate of the SET and the source of NMOS are shorted in the output circuit (second part). The drain current of the SET oscillates periodically with the increase of input voltage signal at the input gate [14]. The analog voltage is used as output signal of the hybrid DAC circuit.

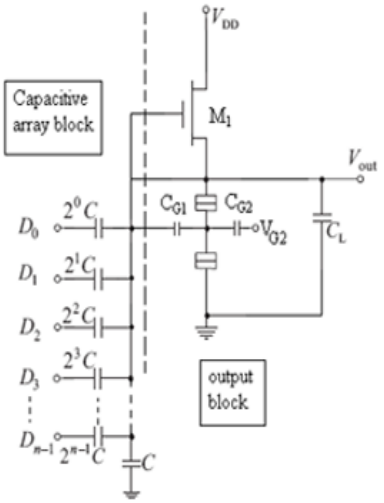

Fig. 4. Schematic of n-bit hybrid SET/MOS DAC circuit

2.2. Simulation results of 4-bit and 8-bit DAC circuits

This circuit is SET/MOS hybrid DAC circuit, which is difficult to simulate using the MOS circuit simulation method or the SET circuit simulation method separately. Therefore the Recursion Relation Model (RRM) with four charge states using OrCAD Capture PSPICE program that is used in the circuit by the double-gate SET simulation model. The parameters of resistances and capacitances are set as follows:

The tunnel junction resistance (R_1,R_2) to be greater than the quantum resistance (~26 kΩ) to confine the electrons in the island; the charging energy of the island capacitance to be larger than the available thermal energy to avoid electron tunneling due to the thermionic emission, namely, $e^2/2C_\Sigma > k_BT$ [14]. Where $C_\Sigma=C_1+C_2+C_{G1}+C_{G2}$ is the total capacitance of the island with respect to the ground, k_B is the Boltzmann's constant, and T is absolute temperature [15].

Compared with pure SET DAC circuit [16],[17], the proposed hybrid SET/MOS DAC uses fewer electronic components, which simplifies the structure of the circuit, increase the operating temperature, enhances the load capability and the signal output scope. Fig. 5 shows the simulation results waveform of 4-bit DAC circuit using Orcad Capture PSPICE. Fig. 6 shows the simulation results waveform of 8-bit DAC circuit using Orcad Capture PSPICE.

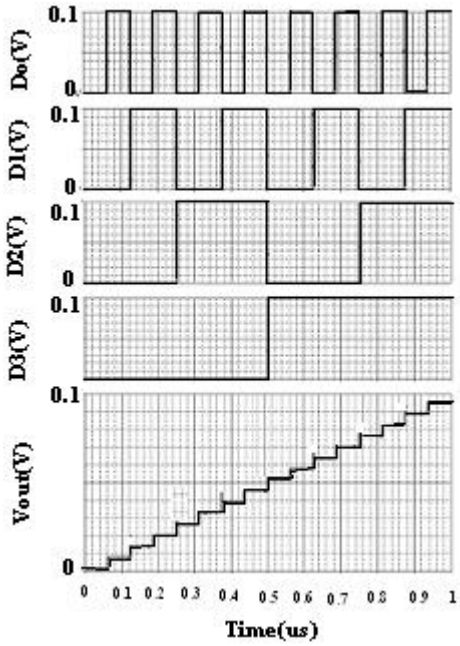

Fig. 5. PSPICE simulation results for the proposed 4-bit hybrid DAC

Compared with DAC circuit in [14]. The improved hybrid SET/MOS DAC uses fewer electronic components, simplifies the structure of the circuit, enhances the load capability and the signal output. The power dissipation of designed 4-bit DAC is 3.25E-11W, which is lower than the previous proposed SET/MOS DAC [14]. Table 1 shows a comparison between the previously reported DAC in [14] and the improved DAC.

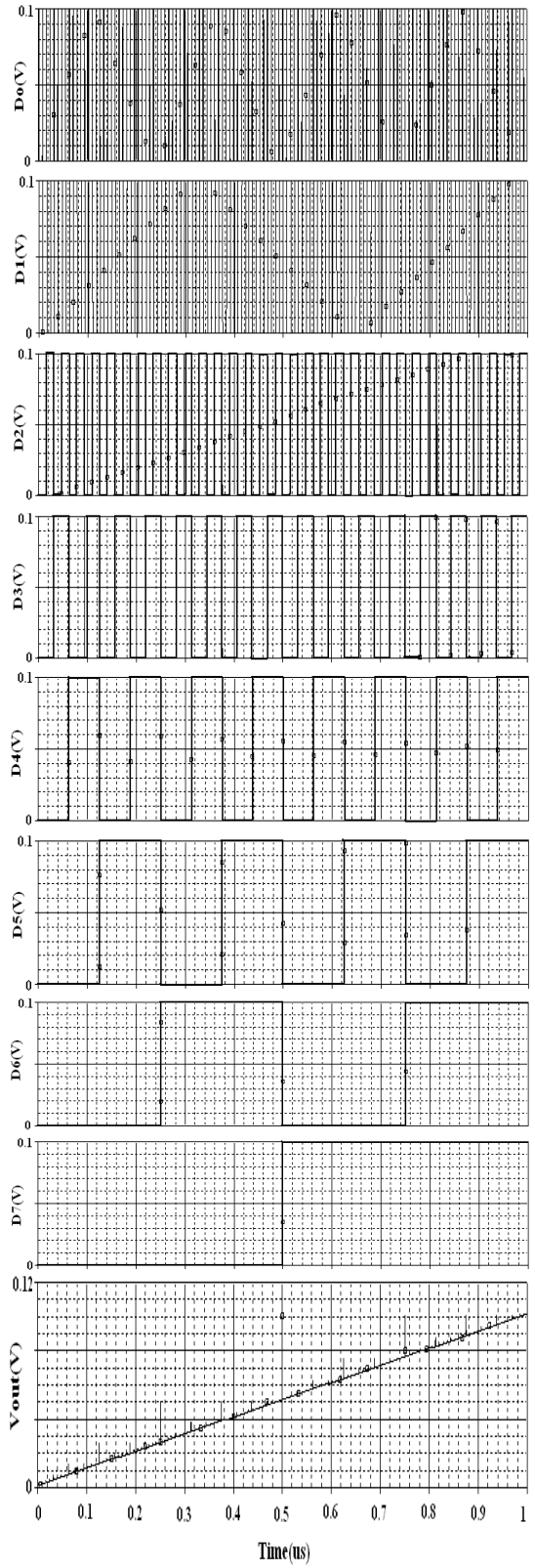

Fig. 6. PSPICE simulation results for the proposed 8-bit hybrid DAC

Table 1. Comparison between the previously reported DAC in [14] and the improved DAC

The simulation parameters	Hybrid 4-bit DAC [14]	Improved DAC
Power supply voltage	0.3V	0.1V
Power dissipation	2.52E-10W	3.25E-11W
Capacitance Array Block (F)	C=1E-12F	C=10E-12F
Capacitive drive capability	several fFs	several hundreds of fFs=500fF
Temperature (K)	100K	20-1000K
Total job time	38.27Sec	15.86Sec
SET parameters	C_{G1}=1.8E-18F C_{G2}=0.64E-18F C_1= C_2=1E-19F R_1=R_2=2E6Ω	C_{G1}=2E-18F C_{G2}=0.7E-18F C_1=C_2=1E-19F R_1=R_2=1E6Ω
NMOS parameters	M_1: L= 150nm W= 30nm Depletion type	M_1: L=150nm W=15nm V_{to}=-0.018V Depletion type

3. ADC using hybrid SET/MOS circuit

3.1. Operating principle for n-bit hybrid SET/MOS ADC circuit

Fig. 8 shows the schematic of an n-bit hybrid SET/MOS ADC circuit, which consists of a capacitive divider and *n* Periodic Symmetric Function (PSF) with the same circuit parameters[18]. The PSF circuit is composed of two cascade circuits that are shown in Fig. 7. The first part is a SET in series with depletion type NMOS (the same as the output circuit of DAC), the second part is a common source amplifier circuit. The ADC operation as follow:

The analog input signal V_{in} is divided by the signal divider into n voltage signals ($V_{in}/2^i$, i= 0,1,2,….n-1). Then, the analog signals are converted into the corresponding binary output signal by the PSF units with the same circuit parameters[14]. Fig. 9 shows the (V_{o1}-V_{in}) waveform of PSF at different temperatures (5, 30, 50, 80, 100K). From the figure as the temperature increase, the output of the first part V_{o1} become smoother.

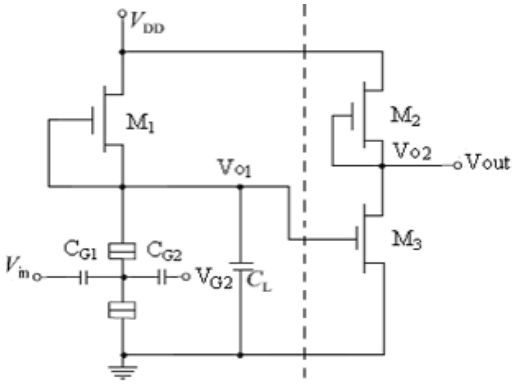

Fig. 7. Schematic of a complementary SET/MOS Periodic Symmetric Function (PSF)

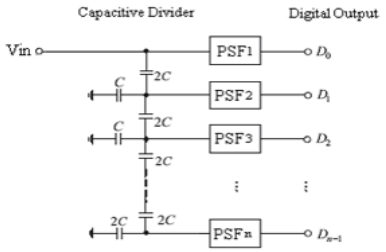

Fig. 8. Architecture for an n-bit ADC

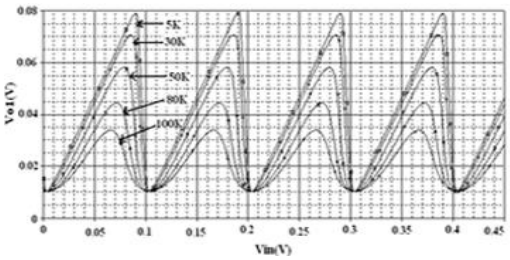

Fig. 9. The waveform of (V_{o1}-V_{in}) under different temperature

3.2. Simulation results of 3-bit and 8-bit ADC circuits

The operating temperature of hybrid SET/MOS device should be chosen carefully, this will adequately embody the performance of SET device and MOS device [14]. Compared with previous proposed SET/MOS ADC [19], the proposed 3-bit ADC circuit has only one power supply and it can operate at higher temperature. Compared with the previous proposed SET-based ADC [8], [11], [20], the proposed hybrid SET/MOS ADC is enhanced in operation temperature from 0K~10K to 144K, heightened the load capability and signal output scope.

Fig. 10 shows the Voltage Transfer Characteristics of SET/MOS Periodic Symmetric Function (PSF) at 100K. Fig. 11 show the simulation results of 3-bit ADC circuit using Orcad Capture PSPICE, the first waveform is the input ramp voltage, the rest of the waveform show the digital output signal D_0, D_1 and D_2. An 8-bit ADC circuit was simulated using Orcad Capture PSPICE. Fig. 12 show the simulation results of 8-bit ADC circuit. Table 2 shows a comparison between the previously reported ADC in [14] and the improved ADC.

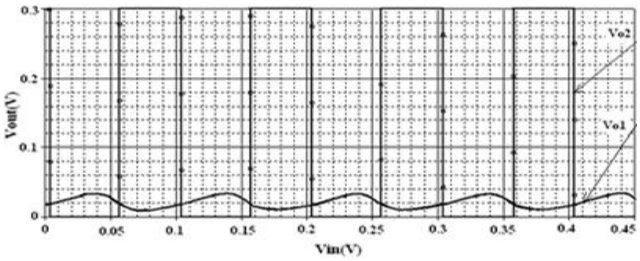

Fig. 10. Voltage Transfer Characteristics of Periodic Symmetric Function (PSF)

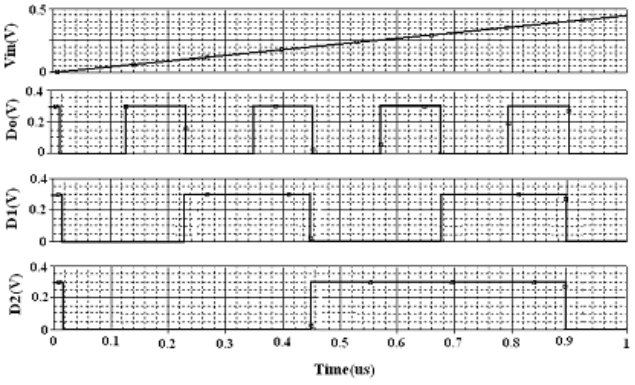

Fig. 11. Simulated waveform of 3-bit ADC Hybrid SET/MOS

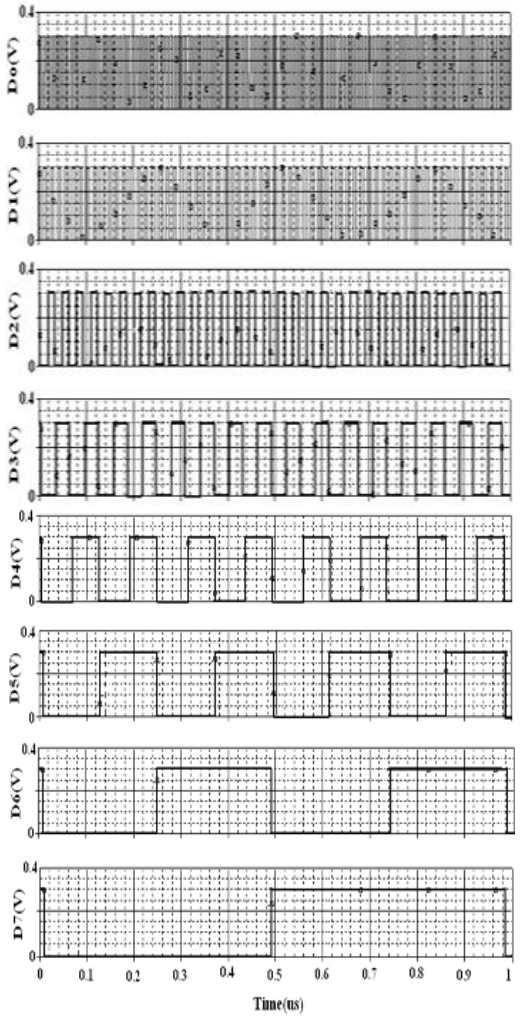

Fig. 12. Simulated waveform of 8-bit ADC Hybrid SET/MOS

Table 2. Comparison between the previously reported ADC in [14] and the improved ADC

The simulation parameters	Hybrid 4-bit ADC [14]	Improved ADC
Power supply voltage	0.3V	0.1V
Power dissipation	2.52E-10W	3.25E-11W
Capacitance Array Block (F)	C=1E-12F	C=10E-12F
Capacitive drive capability	several fFs	several hundreds of fFs=500fF
Temperature (K)	100K	20-1000K
Total job time	38.27Sec	15.86Sec
SET parameters	C_{G1}=1.8E-18F C_{G2}=0.64E-18F C_1= C_2=1E-19F R_1=R_2=2E6Ω	C_{G1}=2E-18F C_{G2}=0.7E-18F C_1=C_2=1E-19F R_1=R_2=1E6Ω
NMOS parameters	M_1: L= 150nm W= 30nm Depletion type	M_1: L=150nm W=15nm V_{to}=-0.018V Depletion type

4. Simulation results of 8-bit ADC circuit using SET

Single Electron Transistor inverter consists of two SETs in series, Fig. 13 shows the circuit diagram for a SET inverter. To simulate a SET inverter with 50% duty ratio, V_G has been adjusted to V_{G1}=0V and V_{G2}=-0.16V [22]. When the upper SET turns on, the lower SET turns off because SET has the inherent Coulomb oscillation characteristics with the period of q/C_g [22]. The circuit parameters are as follows: The supply voltage V_{DD}=10mV, C_{G1}=0.24E-18, C_{G2}=0, the capacitances of tunnel junctions C_1=C_2=1.3E-18, the resistances of tunnel junctions R_1=R_2=1.3E6, T=30K and the load capacitance C_L= 1pF[22].

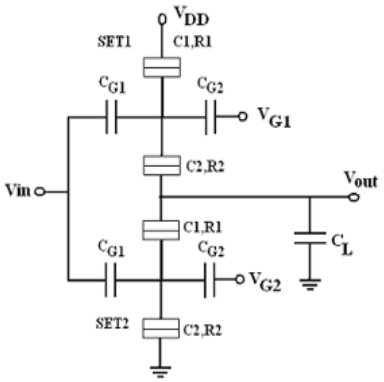

Fig. 13. Schematic of SET inverter [5]

Using SET inverter as a unit circuit, as shown in Fig. 8, an 8-bit ADC architecture is simply implemented with a capacitive divider, and eight SET inverters with the same circuit parameters. In the 8-bit ADC circuit, the analog signal input is divided into $V_{in}/2^i$ where i=0,1,2,3,4,5,6,7 by the capacitive divider, then it is encoded into the corresponding 8-bit digital signals $D_0,D_1,D_2,D_3,D_4,D_5,D_6,D_7$ by the SET inverters. Fig. 14 shows the simulated conversion characteristics of the 8-bit ADC based on SET inverter using Orcad Capture PSPICE.

The comparison of ADC using CMOS, ADC using SET and ADC using hybrid SET/MOS for a 3-bit ADC is presented in Table 3. The switching speed of SET circuits is determined by its RC time constant. The size, speed and power consumption of ADC using CMOS is from [21]. For a 3-bit ADC realized using CMOS one would require 63-MOS transistor components [21], but when the 3-bit ADC is realized using SET, it requires 6-SET transistor and 8-capacitors components and 3-bit ADC using hybrid SET/MOS requires 9-MOS, 3-SET and 8-capacitor. Conversion speed of ADC using SET and ADC using hybrid SET/MOS are equal and faster than CMOS. The power consumption for ADC using hybrid SET/MOS is smaller than ADC using SET and ADC using CMOS.

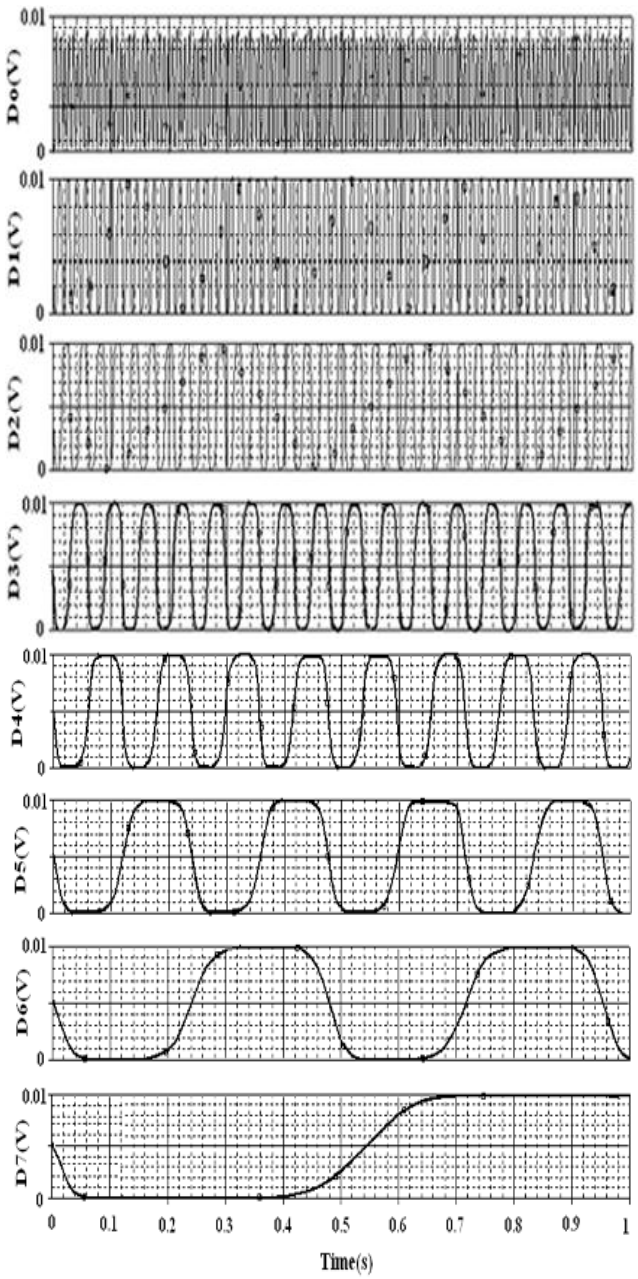

Fig. 14. Simulated waveform of 8-bit ADC using SET

Table 3. Comparison between ADC using CMOS, ADC using SET and the improved ADC using hybrid SET/MOS

Simulation parameters	ADC using CMOS	ADC using SET	ADC using Hybrid SET/MOS
Size	63 MOS Trans. [21]	6-SET 8-capacitor	9-MOS 3-SET 8-capacitor
Speed	250 MHz-1GHz[21]	Approx. 1GHz	Approx. 1GHz
Power Consumption	In range of mW[21]	3.49E-8W	2.92E-10W

5. Conclusion

In this paper, improved hybrid SET/MOS ADC and DAC circuits were implemented and simulated. The improved hybrid n-bit DAC nano-circuits are simulated (for n=4 and 8) using Orcad Capture PSPICE. The performance of the SET/MOS hybrid n-bit ADC circuits were simulated (for n=3 and 8). Also ADC circuits using Single Electron Transistor were simulated (for n=8) using Orcad Capture PSPICE. In our results, the transient operation of hybrid SET/MOS circuit-based DAC is successfully demonstrated at 1000K and ADC at 144K. This performance can be compared with the pure SET circuits, the improved converter circuits have been enhanced in the drive capability and the power dissipation. Compared with the other SET/MOS hybrid circuit, the implemented converter circuits have compact circuit structure, higher integration density, high speed, high load drivability, low current and low power dissipation.

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