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# Modeling and Simulation of a Saturated Core Fault Current Limiter Integrated in a Typical Distribution System Based on PSCAD Environment.

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# Modeling and Simulation of a Saturated Core Fault Current Limiter Integrated in a Typical Distribution System Based on PSCAD Environment

# نمذجة ومحاكاة لمحدد تيار الخطأ ذو القلب المشبع المركب مع نظام توزيع حقيقي باستخدام برنامج PSCAD

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**KEYWORDS:**
*Saturated Core Fault Current Limiter, PSCAD simulation, FCL modeling, Typical Egyptian Distribution*

*الملخص :نتيجة للزيادة المستمرة فى اضافة الاحمال الكهربية و التوسع المتوقع فى محطات التوليد(مثل المولدات الموزعة DG) مما يؤدى بالفعل لزيادة مستويات تيار الخطأ عن المقننات التى تم ضبطها عليه من قبل . و حاليا يوجد عدد من الحلول التقليدية المستخدمة لحل هذة المشكلة مثل استبدال المعدات الموجودة باخرى ذات مقننات اعلى او تركيب ملفات حثية على التوالى او استبدال المحولات وهذا الحل يعد خسارة كبيرة من الناحية الاقتصادية. فى هذا البحث يقدم المؤلفون حلا جديدا وذلك باستخدام محددات التيار فائقة التوصيل ذات القلب المشبع. واعتمد المؤلفون فى نمذجة هذا النظام على برنامج PSCAD ،حيث تمت نمذجة حقيقية لنظام كهربى حقيقى ممثلا فى جزء من الشبكة المصرية بنطا ذو جهد KV11 .وتم تركيب محدد التيار المقترح واضافة مولدات موزعة DG وعمل اخطاء مختلفة على النظام ذات انواع واماكن مختلفة لاختبار النموذج المقترح حيث اثبتت النتائج مدى كفاءته حيث تم بنائه على اساس امكانية ضبط عناصره ليناسب أى حالات اخطاء محتملة*

***Abstract*— Due to load increasing and generation extensions of the electrical networks, the fault current levels may be largely changed. So, the short circuit capacity may easily exceed the installed equipment interrupting capacity such as circuit breakers. Nowadays there are different methods for restoring the fault current normal values. The traditional methods in power utilities consider one of three options: (1) Replace installed equipment with higher rated equipment or, (2) Install series reactors or, (3) Replace the existing transformers with high impedance transformers. In this paper a Saturated Core Superconducting Fault Current Limiter (SCSFCL) will be presented as an efficient method for solving this problem so that replacing existing circuit breaker infrastructure can be avoided or postponed. This paper simulated the SCSFCL based on the PSCAD environment. An 11 kV West Delta Egyptian Distribution System in TANTA region is modeled as a typical system with the proposed simulated model of SCSFCL. The model parameters are adapted by the authors to restore the fault current levels as their values before the integration of the Distributed Generation (DG) units. The obtained results ensure that the model is easily used in other distribution systems. The results show also that the model performances can meet utility's needs in mitigating fault current at all types of fault and different fault positions**

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## I. INTRODUCTION

Egyptian utility has to increase its generation sources of the electricity to meet the increasing of load demand. The objectives are to add 4.3GW in 2-3 years to reach 45GW by 2022 [1]. Due to the expected annual

increasing of the grid, the short circuit fault levels will be increased and so the protection devices must be readapted [2]. Nowadays there are many traditional methods for minimizing the problems associated with the increasing of the fault current such as splitting busbars, installing series reactors, replacing equipment with higher rated equipment and replacing the existing transformers with high impedance transformers [3,4]. These traditional approaches may result in bad effects on the flexibility and the stability of the power grid. Among of these methods the Fault Current Limiter (FCL) was proposed in many researches [5-8].

In South Africa, the utilization of a resistive Superconducting Fault Current Limiter (SCFL) was compared against three traditional fault current limiting options. This comparison shows that the high capital cost of the resistive SFCL is the main disadvantage against its main advantage of reduced operating cost over a service life of 25 years. But this conclusion may not be valid for other types of fault current limiters [3].

Also, in case of high voltage DC, (100 kV or more), the resistive SFCL cannot be used because of increasing manufacturing technology problems [4]. So, SCSFCL has become one of the leading modern commercial fault current limiting devices in AC and DC applications. SFCL is considered as an effective solution because of its fast response for fault current and low power loss during normal operation.

In this paper the authors use a SCSFCL to be integrated in a typical distribution system. The case study of typical system in Egypt is presented with different 7 fault types and different fault positions with the proposed SCSFCL model. The proposed SCSFCL is modeled and simulated using PSCAD program. Present paper is divided to five sections: the operation of SCSFCL is presented in section II. The modeling and simulation of the proposed model was presented in section III. At the end of the paper the main results and conclusion were found.

## II. SCSFCL OPERATION

*A.* The FCL is divided to the externally activation type and the self-triggered one. The SFCL is considered as a self-triggered type. This type contains non quench and quench techniques. The SCSFCL used in this paper is an example of the non-quench technique [6, 7, and 9]. The idea of SCSFCL was suggested by B. P. Raju group in 1980's. Normally, it is connected in series with the load current. It operates as a low impedance in normal operation and a high impedance in faulted operation due to the change in permeability between saturated and unsaturated states of the core material.

*B. The main components of SCSFCL are presented as follow (Figure 1):* Fig. 1 Single-phase SCSFCL [5]

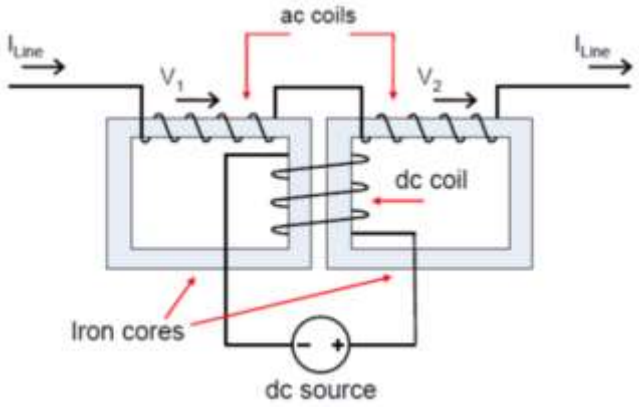



Fig. 1 Single-phase SCSFCL [5]

- AC coils and DC superconductor coil which has high capability to supply permanent ampere-turns to magnetize the iron-cores without significant losses [6].
- DC current supply adjusted to keep the iron-cores normally at the deep saturation region of the B-H curve (Figure 2).
- Two iron-cores used for cancelling the electromotive forces induced by the AC windings through the transformer effect on the superconducting DC coil.

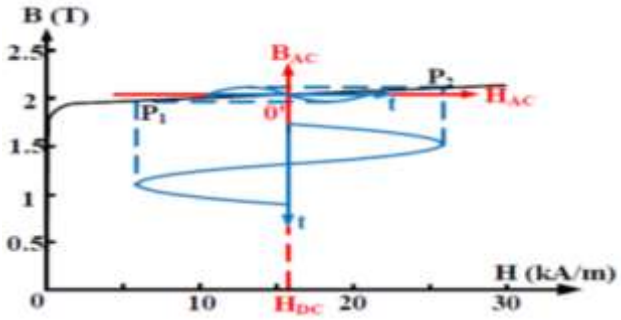



Fig. 2 SCSFCL B-H curve [7].

*C. The SCSFCL principle of operation is presented as follow:*

- The flux variations in the normal operation are very small, as shown in Figure 2, BAC is located normally between points P1 and P2 which means that the core normally operates in deep saturation region.
- During fault state in the power grid side, the high fault current tries to desaturate the iron cores. It also induces, at the same time; high voltage on the DC coils, which reduces the level of the fault current [6].

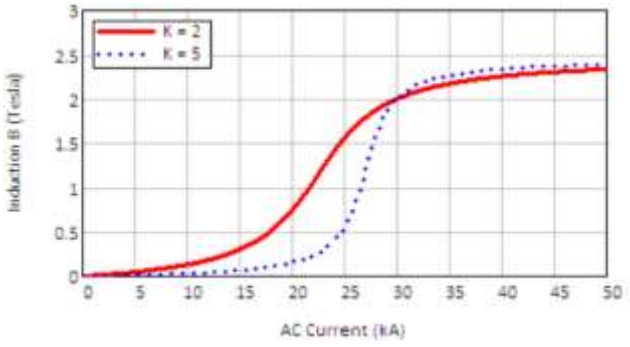
The flux linkage magnetic field in the core section seen by one

AC coil is obtained by the following equation [8]:

$$B(i_{ac}) = \frac{-2\,B_{sat}}{1+tan^{-1}\left(K\pi-\frac{\pi}{2}\right)}\left(1+tan^{-1}\left(K\frac{\pi}{I_{max}}(I_{max}-i_{ac})-\frac{\pi}{2}\right)+2\,B_{sat}\right) \quad (1)$$

where $i_{ac}$ is the AC instantaneous line current, $I_{max}$ is the line current fully saturates the cores, at which the average magnetic field is $B_{sat}$ , and K is a constant determines the range of line currents where the magnetic state of the cores are actively changing from saturated to unsaturated.

For a value of $B_{sat}$ = 2.2 Tesla, $I_{max}$ =30kA, the variation of flux density B caused by AC operating current $i_{ac}$ is shown in Figure 3.




AC current (KA)
Fig 3 Variation of B with Operating Currents [8].

According to Innopower (Superconductor Cable Co., Ltd., China) [6], the location of FCL plays a high effective parameter to reduce the value of fault current. Figure 4 summaries the different possibility of the FCL locations.

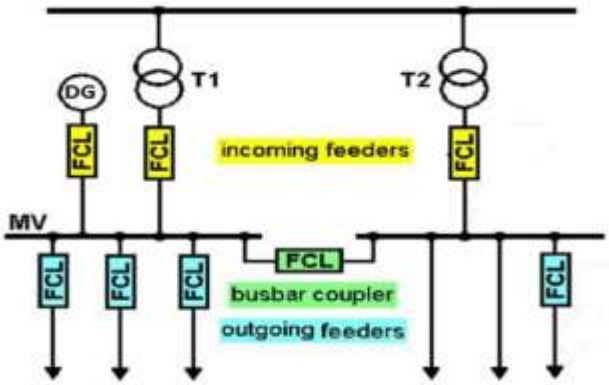



Fig 4 Possible Practical FCLs Locations [5].

SCSFCL design equations were presented in details in [10, 11]. It is a multi-variable optimization problem which should find the solutions of the following problems [12- 15]

- Damages on the DC magnetization circuit according to the very high induced voltage during fault.
- The device heavy weight and large size.
- The two iron cores are not identical which causes that their magnetic flux is not cancelled during fault.
- The AC cores must operate in saturated region in the normal operation to have sufficiently low impedance during power transmission.

## III. SCSFCL MODELING AND SIMULATION

The SCSFCL model consists as follow (Figure 5):

1. An Inductor (L) which is wound with a High Temperature Superconductor (HTS) wire and cooled by a separate cooling apparatus. It provides an effective way of mitigating fault currents within the first cycle because the current cannot change instantaneously in the inductor.
2. Thyristor (Th) inserted to simulate the harmonic effect in the actual SCSFCL.
3. Linear variable impedance (R) which simulates the behavior of switching on of the mechanical switch and the corresponding switching voltage arc.

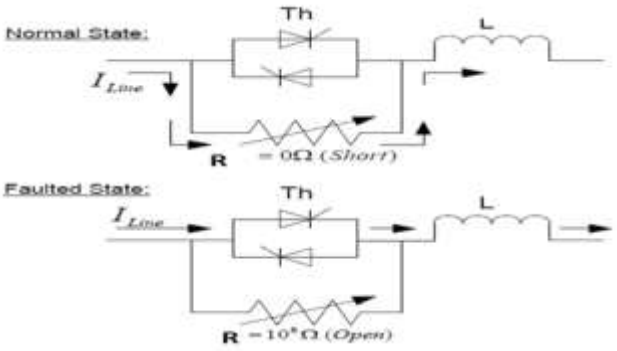



Fig 5 Model in Normal and Faulted States [16].

Figure 6 represents the configuration of the distribution system at Tanta city as a part of the Egyptian 11 kV West Delta distribution system which consists of 15 bus. Its data are presented in Table (1)

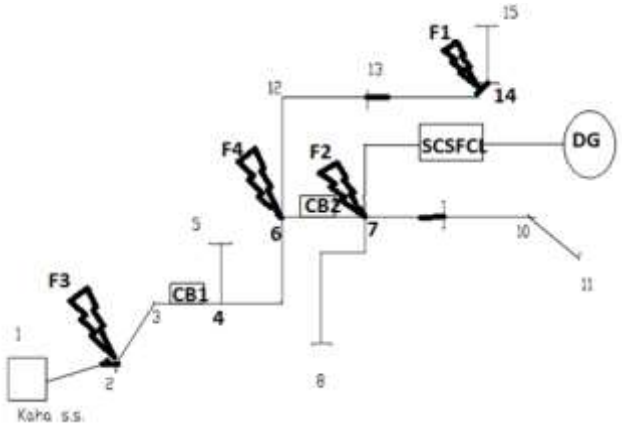



Fig 6 Single Line Diagram of the Test System [17].

The test system was described in details in [17]. The location of the added DG unit is assumed at bus 7. The DG is modeled as an ideal source which their resistance and inductance values are 0.08829 Ω 15.92mH respectively. Four fault positions (F1, F2, F3 and F4) will be studied. At each fault position the currents through circuit breakers 1 (CB1) are calculated and compared with the cases before inserting the DG and after inserting the SCSFCL in series with the DG [17].

Figure 7 describes the proposed model simulated which is developed based on PSCAD® X4 (v4.5.0) professional simulation software. It is used to study and analyze the studied system.

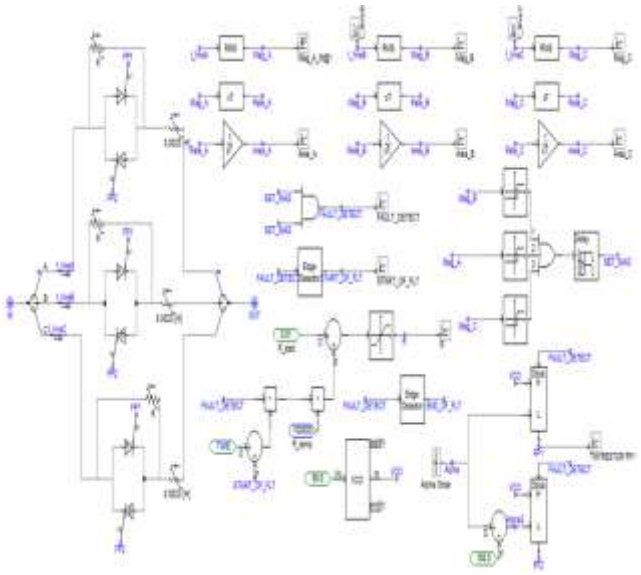


Fig 7 Proposed SCSFCL PSCAD Model

TABLE 1
TEST SYSTEM DATA

| from | to | KM line length | LINE PARAMETERS R Ω/km | X Ω/km | Y/2 |
|---|---|---|---|---|---|
| 1 | 2 | 0.078 | 0.163 | 0.0892 | 0.00007 |
| 2 | 3 | 0.85 | 0.266 | 0.0949 | 0.00005 |
| 3 | 4 | 0.22 | 0.569 | 0.1062 | 0.00004 |
| 4 | 5 | 0.05 | 0.569 | 0.1062 | 0.00004 |
| 4 | 6 | 0.33 | 0.569 | 0.1062 | 0.00004 |
| 6 | 7 | 0.2 | 0.569 | 0.1062 | 0.00004 |
| 7 | 8 | 0.04 | 0.569 | 0.1062 | 0.00004 |
| 7 | 9 | 0.65 | 0.266 | 0.0949 | 0.00005 |
| 9 | 10 | 0.15 | 0.569 | 0.1062 | 0.00004 |
| 10 | 11 | 0.1 | 1.113 | 0.1172 | 0.00003 |
| 6 | 12 | 0.44 | 0.569 | 0.1062 | 0.00004 |
| 12 | 13 | 0.15 | 0.266 | 0.0949 | 0.00005 |
| 13 | 14 | 0.45 | 0.266 | 0.0949 | 0.00005 |
| 14 | 15 | 0.2 | 0.266 | 0.0949 | 0.00005 |

*A. Adaptation of the proposed SCSFCL inductance.*

It is clear that the value of the fault current level is changed so that the protection devices should be readapted or replaced. This paper will use SCSFCL to solve this problem. A three phase to ground fault is assumed occurred at the studied system (at position F1) started at time t=1 sec with duration of 1 sec. The obtained results are shown in Figure 8 (Before inserting the DG) and Figure 9 (after integrating the DG).

Table 2 presents a summary of peak currents in kA through CB1. From the Table 2, the best inductance value is 0.23H which regulates the values of the current after and before inserting the DG are the same. The effect of the variations of inductance L of the fault current limiter are shown in Figures 10-13.

TABLE 2 PEAK CURRENTS SUMMERY

| Case | If (kA) |
|---|---|
| Before DG | 8.3 |
| With DG | 4.5 |
| With DG&SCSFCL (L=0.23H) | 8.3 |
| With DG&SCSFCL (L=0.023H) | 8.2 |
| With DG&SCSFCL (L=0.0023H) | 8.0 |
| With DG&SCSFCL (L=0.00023H) | 6.0 |

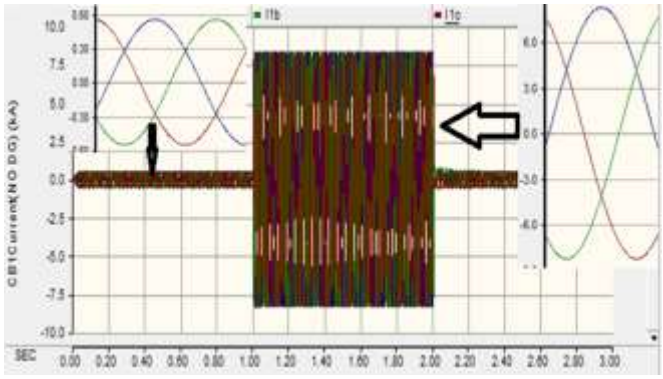


Fig 8 CB1 current before inserting the DG (at F1)

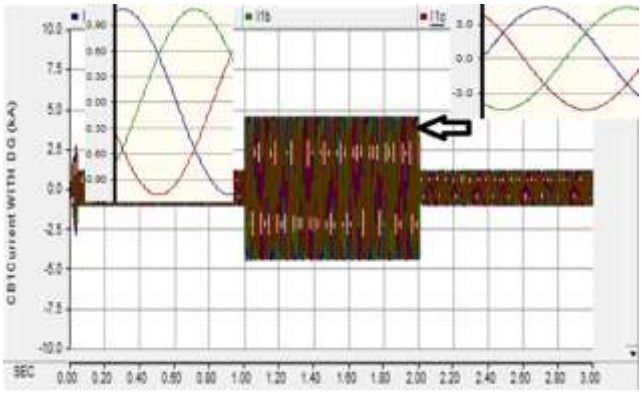


Fig 9 CB1 current after inserting the DG (at F1)

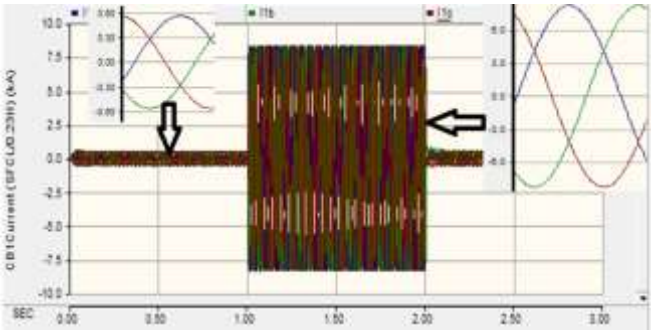


Fig 10 CB1 current with DG&SCSFCL (L=0.23H) (at F1)

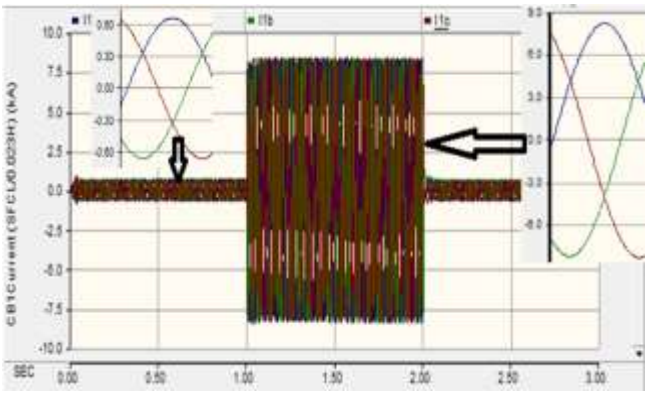


Fig 11 CB1 current with DG&SCSFCL (L=0.023H) (at F1)

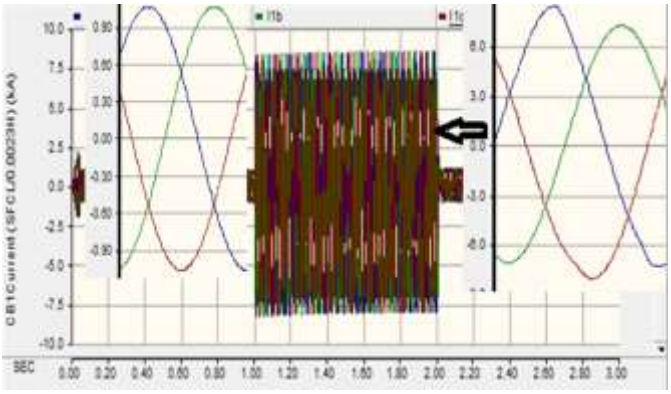


Fig 12 CB1 current with DG&SCSFCL (L=0.0023H) (at F1)

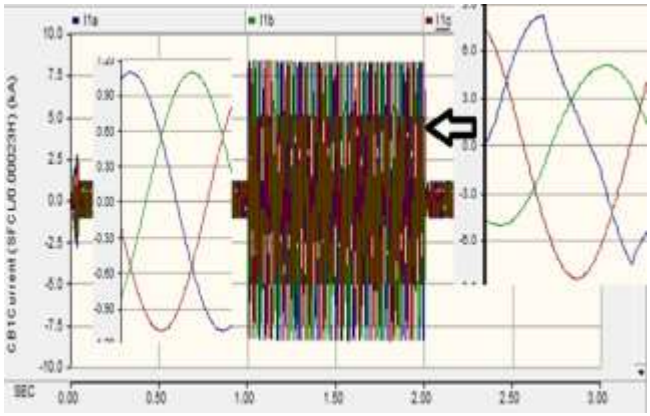


Fig 13 CB1 current with DG&SCSFCL (L=0.00023H) (at F1)

B. Performance verification of the used model (L=0.0023H)

For testing the behavior of the SCSFCL during the fault, there is a device element which measures continuously the load current and compares it with reference value. In case of any fault, the device will detect it and send a signal to the resistance R to be increased gradually. At the same time the thyristors TH operate to limit the faulted current with the inductance L, as shown in figure 14.

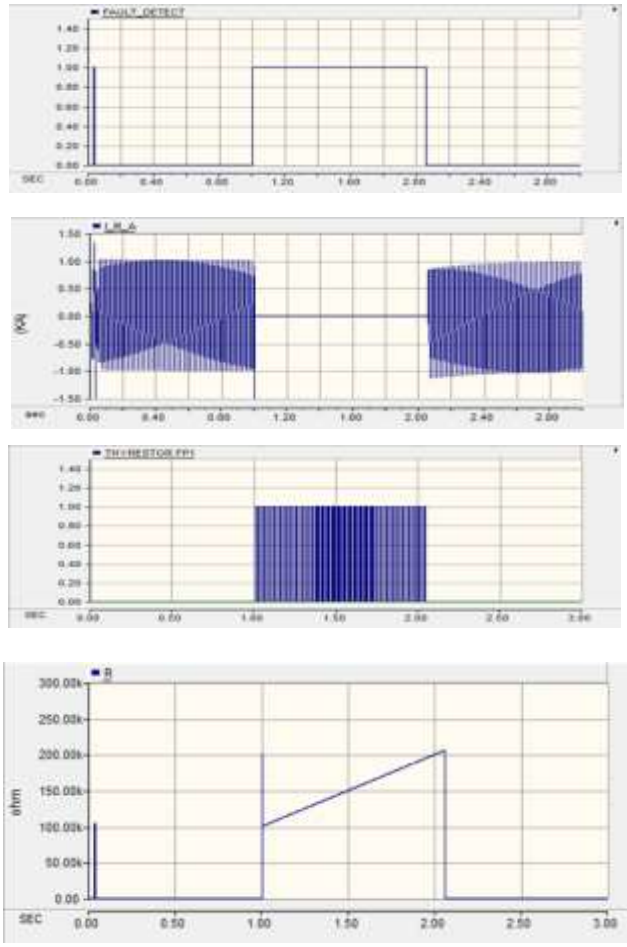


Fig 14 SCSFCL behavior (A-state of fault. B-resistance current. C-operation thyristor state. D- Resistance variation)

## IV. Effect of Fault Types and Locations

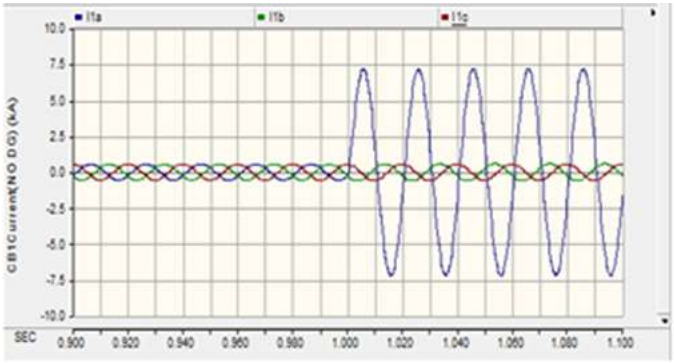
The proposed model is used to study the effect of variation of the fault types and their locations the considered paper test system (Figure 6). The DG unit is always at bus 7. There will be six different cases will be studied as described in details in Table 3. For each case the CB1 currents are measured before and after inserting the DG and compared with the values with existence SCSFCL.

TABLE 3 PEAK CURRENTS THROUGH CB1 IN KA

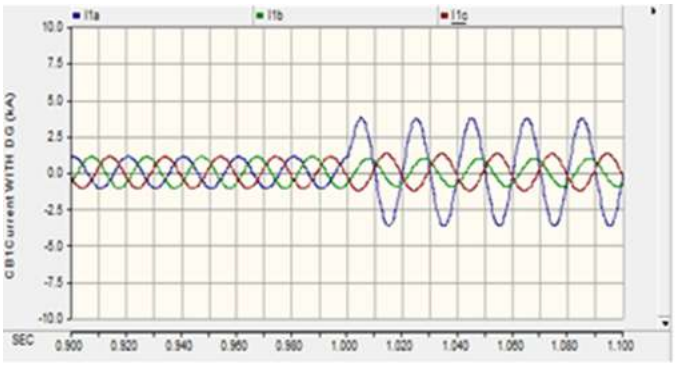
| Case number | Fault location | Fault type | Before DG $I_1$ | With DG $I_2$ | DG + SFCCL $I_3$ | Error (I3-$I_1$/$I_3$) *100% |
|---|---|---|---|---|---|---|
| 1 | F1 | LG | 7.005 | 3.750 | 7.010 | 0 |
| 2 | | 3LG | 8.500 | 4.500 | 8.502 | 0 |
| 3 | | 2LG | 7.502 | 4.004 | 7.505 | 0 |
| 4 | F2 | 3LG | 10.000 | 10.000 | 10.000 | 0 |
| 5 | F3 | 3LG | 0 | 8.800 | 6.250 | 100 |
| 6 | F4 | 3LG | 14.000 | 14.000 | 14.000 | 0 |

From the obtained results shown in Table 3, the proposed SCSFCL model is capable to restore the CB1 currents as before adding the DG units in all different cases by nearly 100 % efficiency. Except the case 5 where the current I1 before inserting the DG equals zero because the system is radial and the fault occurs at F3 before the CB1 then no current will be flow.

The currents waveforms for case 1 are shown in Figure 15.




Before DG insertion case




After DG case

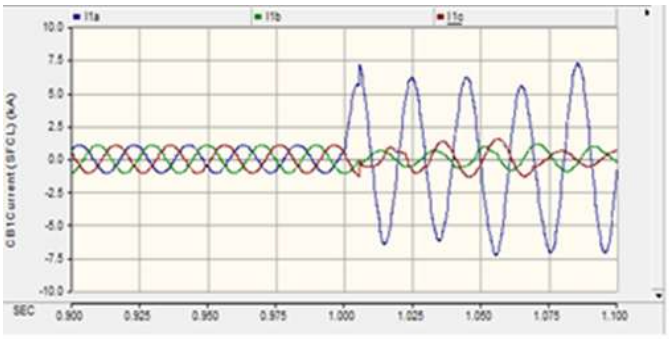



Fig 15 CB1 current waves before DG, after DG, after DG+SCSFCL (case 1)

## V. Conclusion

This paper introduced an efficient solution of the problem of increasing the fault current short circuit levels in the electrical grid due to their extensions by using a proposed SCSFCL. The proposed SCSFCL was modeled and simulated in PASCAD environment. An 11 KV west delta Egyptian distribution system Tanta region was modeled as a typical network with the proposed simulated model. The variation of FCL inductance was analyzed to find the proposed value. The model parameters were adapted by the authors to restore the fault current levels to their values before the integration of the DG. Six different cases are simulated and discussed to test the system. The proposed FCL was capable to mitigate the faults current level to be nearby their values without DG. The obtained results ensure that the model is easily used in other distribution systems. The results show also that the model performances can meet utility's needs in mitigating fault current at all types of fault and different fault positions.

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